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# ASMC 2026

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# Analysis of Resistance Performance of High Dose Boron Doping

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**Co Authors: Bohesharvind Naraiyanan Murthi, Chen Hank, Zhang Wan Chun & Rubin Leonard**

## Presenter's Biography



**Bohesharvind  
Naraiyanan Murthi**  
Process Development  
Engineer



- Bachelor Degree (Hons.) in Chemical Engineering (USM 2022)



- Joined Infineon Technologies (Kulim) Sdn. Bhd. in Sep 2022.
- 4 years of experience in the semiconductor industry.
- Responsible for qualifying next-generation high-current implanters (Si Purion H200 RT and Si Purion H200 Hot).
- Responsible for providing process support in transfer and development projects for Si high-voltage diode and IGBT technologies, with additional support for SiC MOSFET technologies.
- Involved in multiple projects focused on cost reduction, yield improvement, process stability enhancement, and excursion prevention.



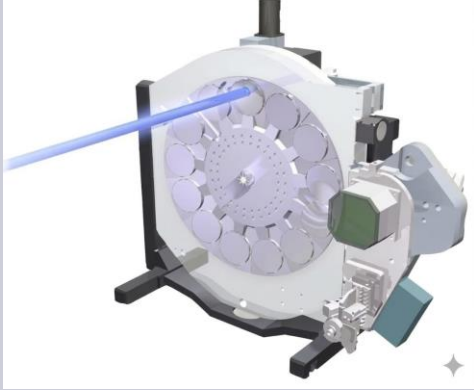
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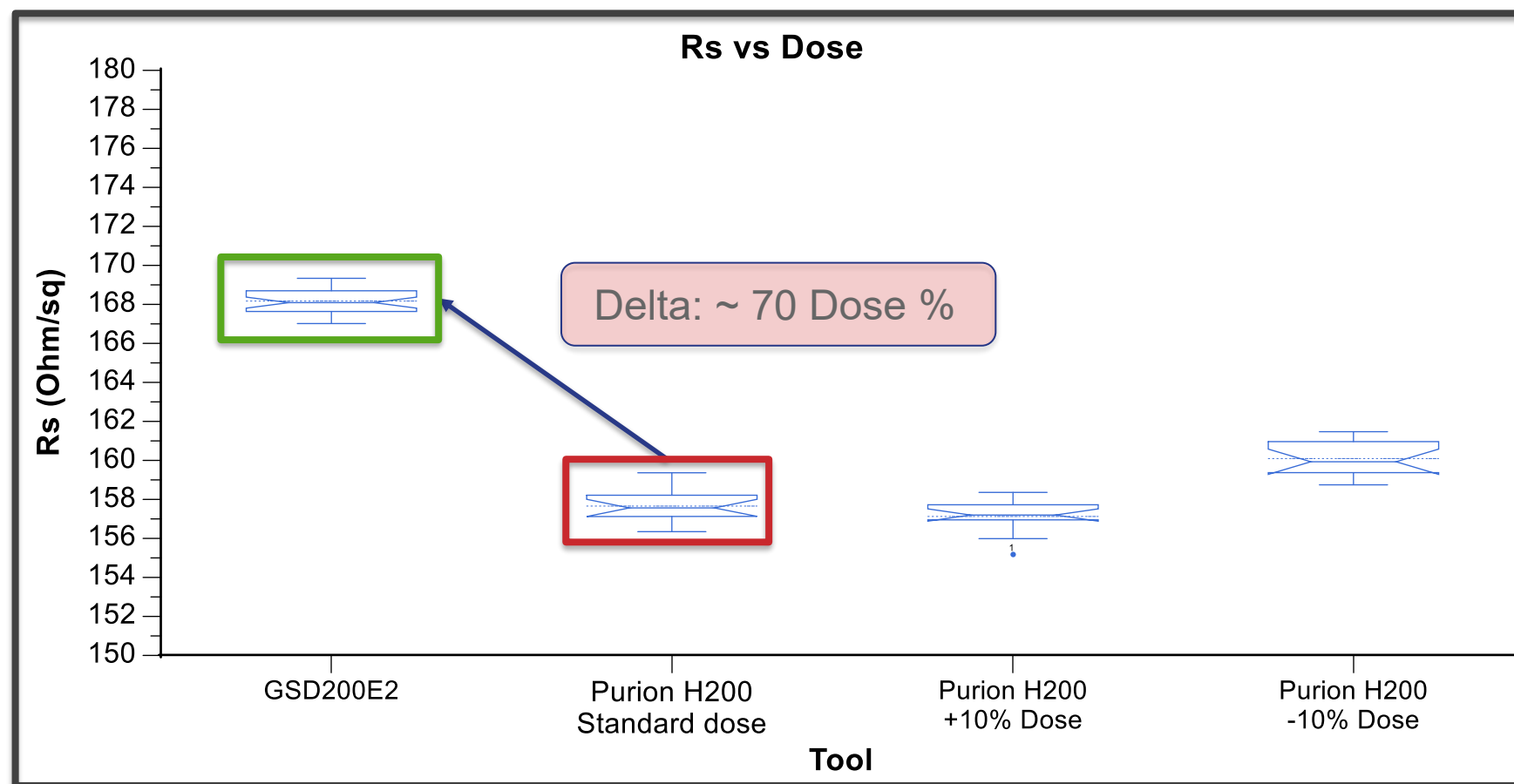
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# Introduction

- Single wafer high current implanters are replacing 13 wafer high current batch implanters due to:
  - Reduced particle contamination
  - Improved yield
  - Extensive development activity
  - Improved tool up time
  - Precise and uniform process enabled by a different beam scanning system [1]
  
- This study qualifies a high dose, low energy boron implant in polysilicon using the Purion H200.
  - Reference tool: GSD200E<sup>2</sup>
  - Conditions: B+/15keV/8.50×10<sup>15</sup> atom/cm<sup>2</sup>/7°
  - Key parameter: Sheet resistance (R<sub>S</sub>)
    - Units: Ohms/sq

Tool model	Axcelis Purion H200	Axcelis GSD200E <sup>2</sup>
Tool type	Single wafer implanter	13 wafer batch implanter
Horizontal scanning	Spot beam is scanned and parallelized magnetically	Spot beam is directed onto a processing disc that spins mechanically at high speed
Vertical scanning	Vertical mechanical scanning of the platen	Vertical mechanical scanning of the process disc
Pad angle	None	5° between wafer pedestal and the disc surface → differential channelling
Illustration		

# Introduction



- **Problem statement:**

- Single wafer implanter demonstrates lower sheet resistance on the polysilicon in comparison to the batch wafer implanter

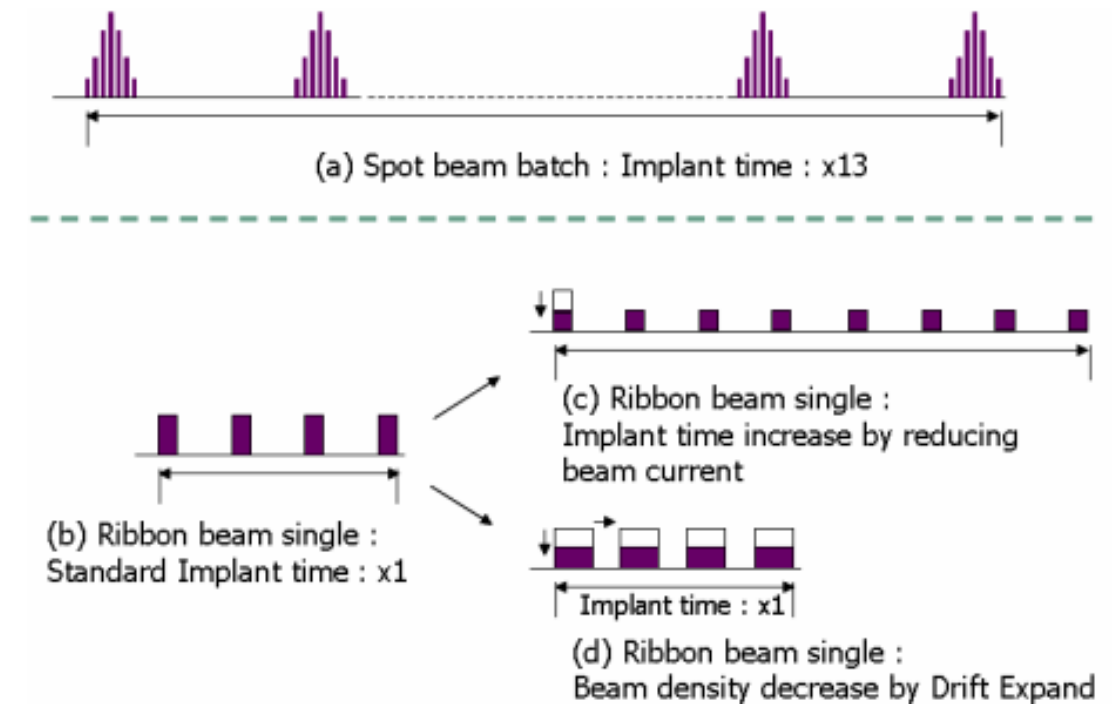
- **Objective:**

- Match the sheet resistance performance within 1 sigma difference with minimal recipe changes
- Enable the single wafer implanter without compromising productivity
- Allow a flexible loading option for the operators to run this product across both the tool types

# Introduction

## Previous Literature: Dose rate effect

- Process matching between a high current single wafer implanter (ribbon beam) and a high current batch wafer implanter (unscanned spot beam) [2]
  - Single wafer implanters have a higher dose rate due to the differences in end station scanning architecture
  - Higher dose rate delivered by the single wafer implanter alters the amorphous layer thickness.
    - Affecting dopant diffusion, activation, and clustering during annealing



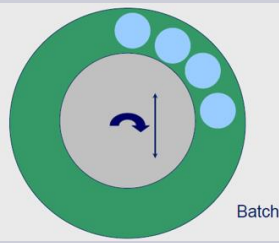
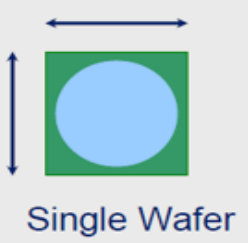
$$\text{Dose rate} = f \left( \frac{\text{Beam current}}{\text{Beam size}} \right)$$

The diagram includes a green arrow pointing down to 'Dose rate', a blue arrow pointing down to 'Beam current', and a yellow arrow pointing up to 'Beam size'.

# Introduction

## Present study:

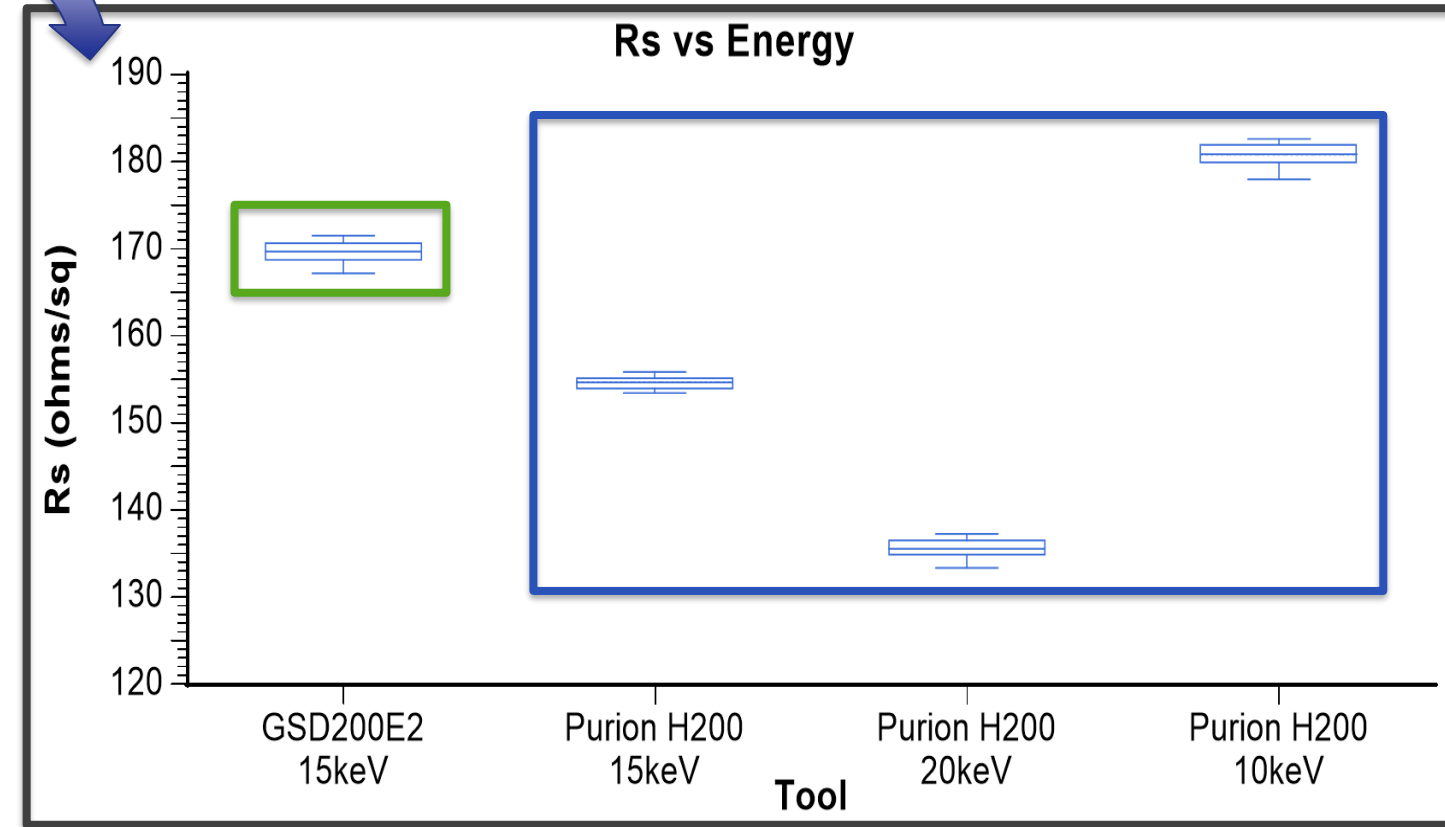
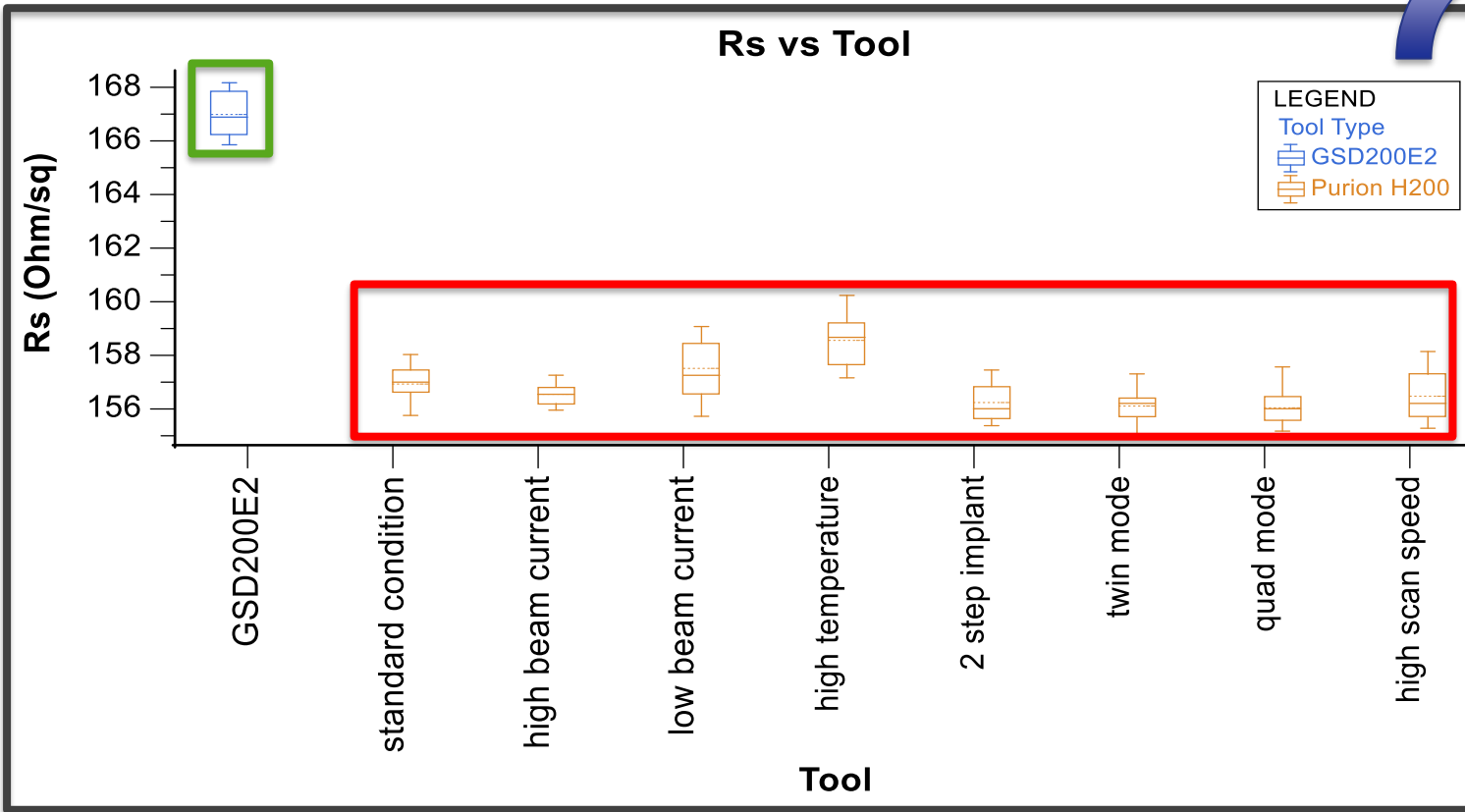
- Both tools use a spot beam, but the differences are (1) maximum number of wafers per batch; (2) beam scanning rate; (3) dose rate (beam density effect); (4) implant area
- These differences may have contributed to the observed mismatch.

Tool type	Wafer per batch	Horizontal scanning rate	Beam Density	Implantation area
Batch wafer implanter	13	Horizontal: 1200 rpm (20 Hz)	~ 9 mA/m <sup>2</sup>	~ 6486.8 cm <sup>2</sup> 
Single wafer implanter	1	Horizontal: 80 Hz	~ 78 mA/m <sup>2</sup>	~ 770.0 cm <sup>2</sup> 

$$t = \frac{q\Phi nA}{I}$$

- $q$  is one electronic charge
- $\Phi$  is the implant dose
- $A$  is the implantation area
- $n$  is the charge state
- $I$  is the beam current
- $t$  is the implantation time

# Introduction



- DOE splits: beam current, chiller temperature, implant mode, and vertical scan speed
- Outcome: unsuccessful

- **Scope**

- Match the sheet resistance performance within 1 sigma by optimizing energy

- Energy split
- Outcome: energy splits had a significant impact on Rs

# Experimental Setup

## Experiment

- Analysis on test wafer: TEM, SIMS, SRP & R<sub>S</sub>
  - Layer stack (from top surface): 5 nm oxide, 200 nm poly, 30 nm oxide & Si substrate
  - Annealing conditions (RTP): 1047°C, 9 secs & N<sub>2</sub> ambient
- Analysis on product wafer: R<sub>S</sub>
- DOE split for on both the wafer types as shown below

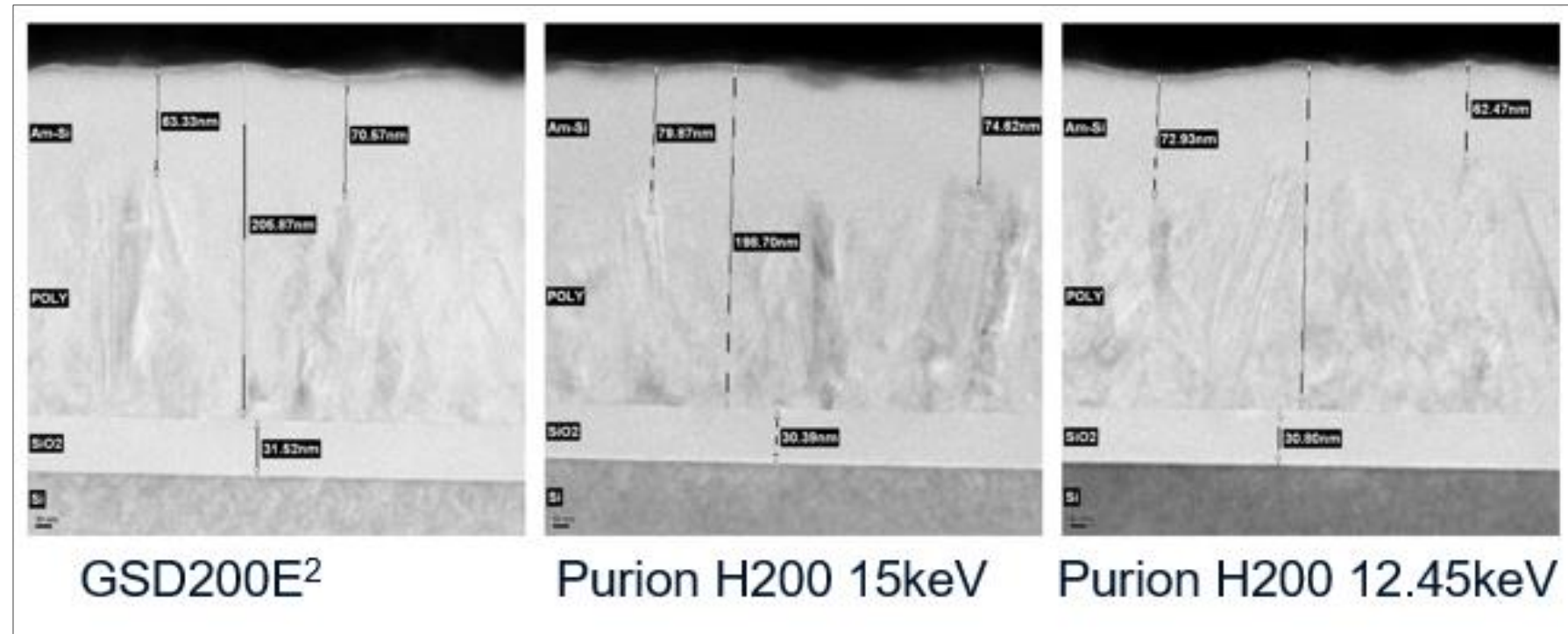
DOE splits	Tool Type	Implant Energy	Anneal
1	Batch wafer implanter	15 keV	No
2	Single wafer implanter	15 keV	No
3	Single wafer implanter	12.45 keV	No
4	Batch wafer implanter	15 keV	Yes
5	Single wafer implanter	15 keV	Yes
6	Single wafer implanter	12.45 keV	Yes

Note:

- 1) RS measurement was done on annealed sample only
- 2) SRP measurement was done on annealed samples only
- 3) TEM measurement was done on as-implanted sample only
- 4) SIMS measurement was done on both sample types

# Results and Discussion (test wafers)

## TEM analysis (as-implanted)

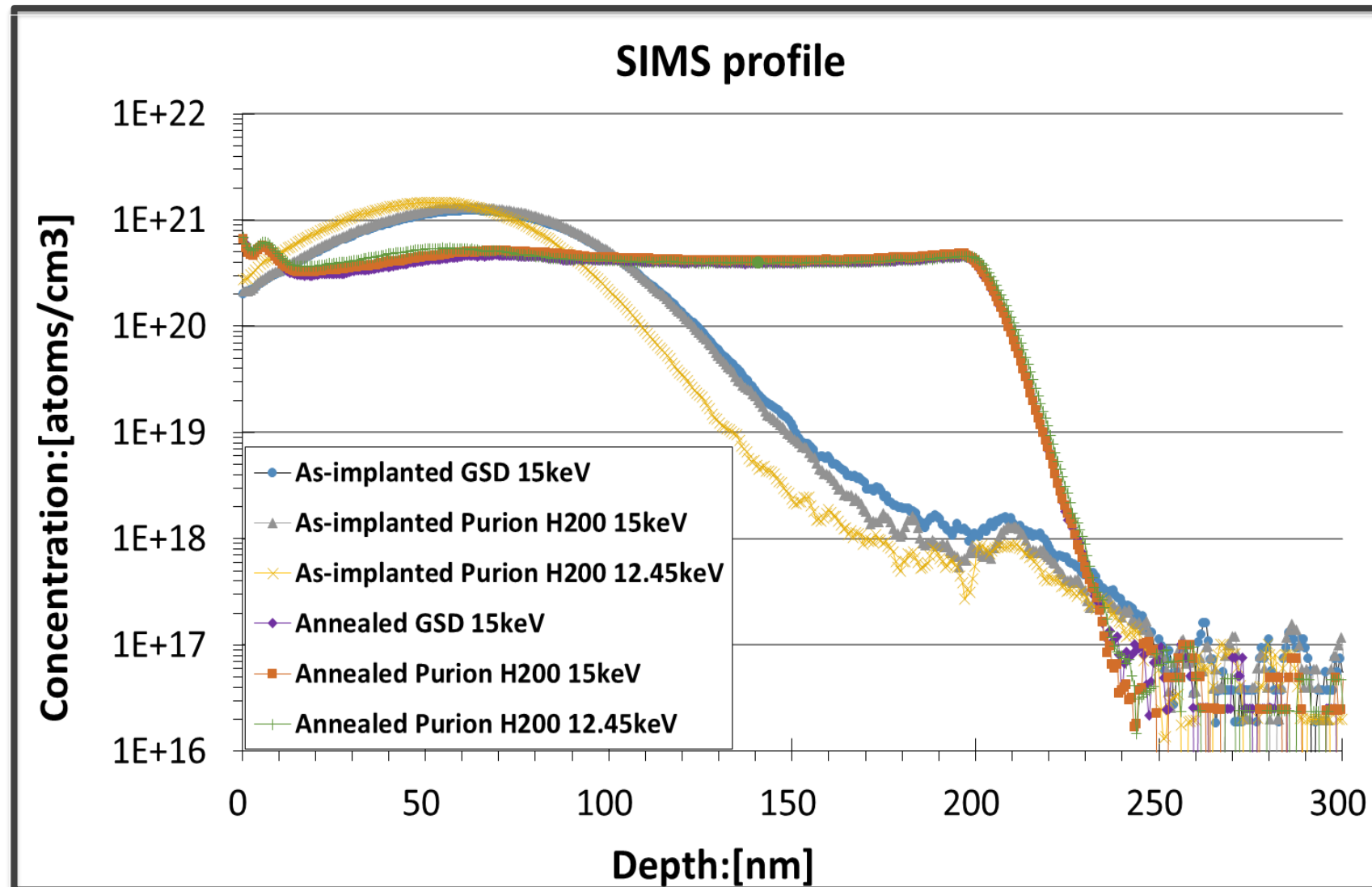


Tool type	Energy (keV)	Average amorphous layer thickness (nm)
Batch wafer implanter	15	66.95
Single wafer implanter	15	77.25
Single wafer implanter	12.45	67.70

- Why does a single-wafer implanter produce a thicker amorphous layer?
  - Higher beam density
    - shortened defect diffusion and less recombination of mobile defects
    - shorter relaxation period of mobile defects
    - damage builds up and overlaps at a faster rate [3]
  
- Why does reducing the ion energy match the amorphous-layer thickness?
  - Lower kinetic energy
    - Lower average projected range
    - fewer collision/scattering event
    - lower integrated damage [4]

# Results and Discussion (test wafers)

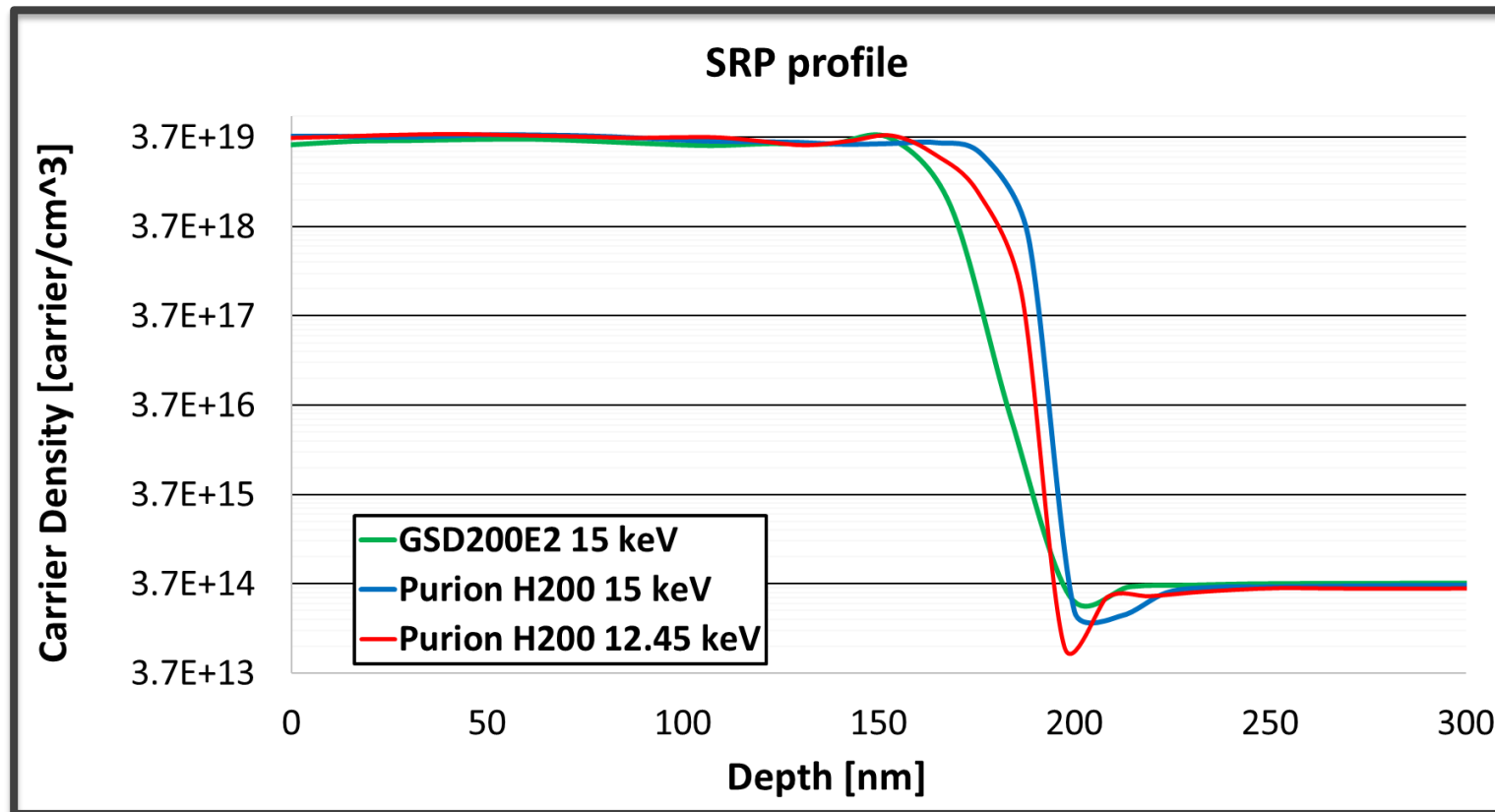
## SIMS Analysis (as-implanted + annealed sample)



- As-implanted sample:
  - Why does the single-wafer implanter show a slightly shallower channeling tail?
    - Higher beam density
      - faster damage build up
      - block channels slightly more for subsequent ions [3]
- Annealed sample:
  - Why don't we observe significant differences in the boron profiles among all three peaks, but a flat tail region in the poly?
    - Grain boundary + excess interstitials
      - higher diffusion coefficient + lower activation energy
      - improved diffusion rate especially at high temperature [6,7]
    - Oxides are introduced to avoid out diffusion of boron from poly [6]

# Results and Discussion (test wafers)

## SRP analysis (annealed)

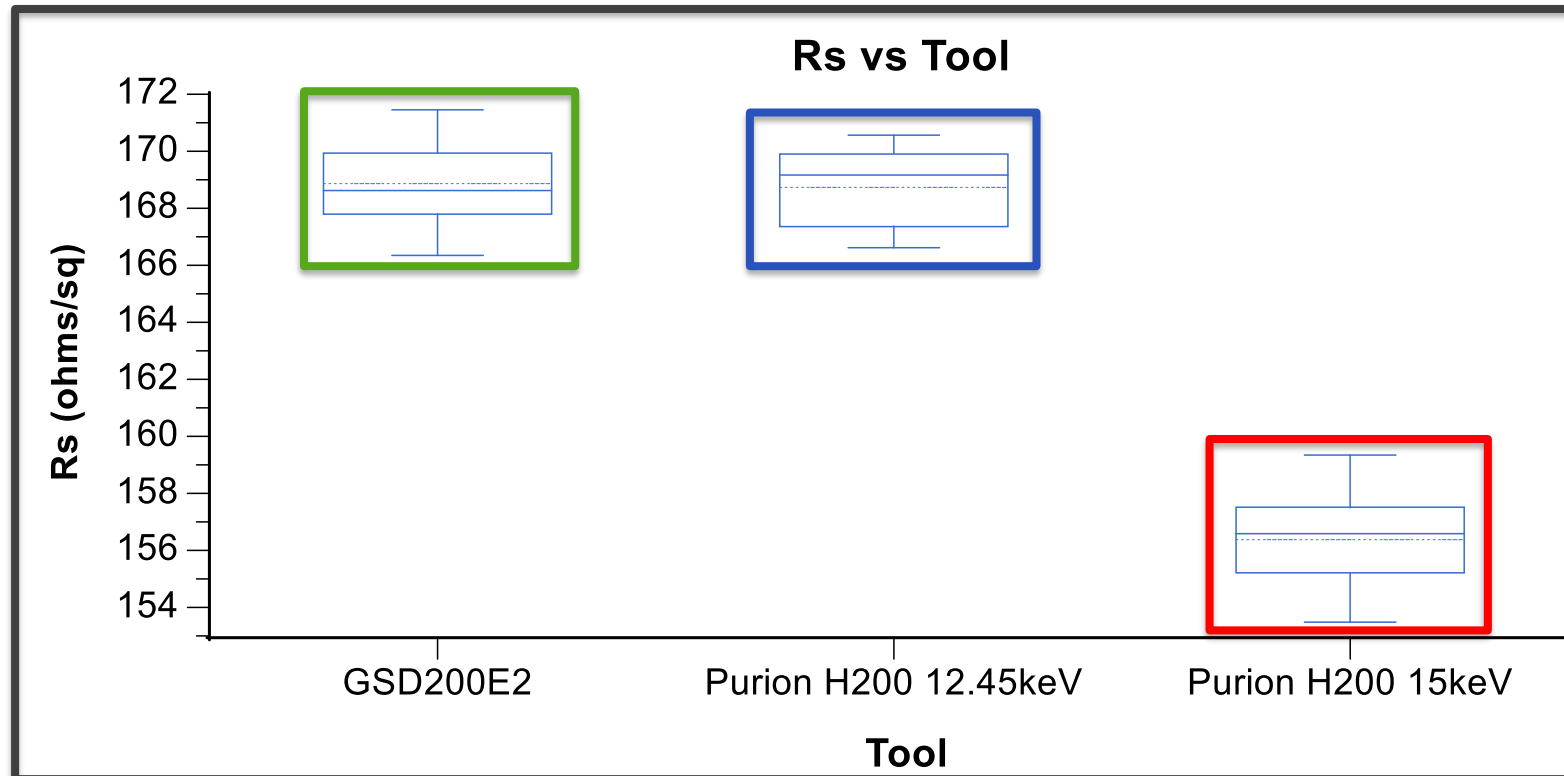


- Why does single wafer implanter demonstrate better activation percentage?
  - Greater amorphous layer thickness
    - more activation via solid phase epitaxy (lower activation energy)
    - better electrical activation [5]
  - Greater amorphous layer thickness
    - fewer end of range (EOR) defects at 150 nm to 200 nm
- Why does reducing the ion energy reduce the activation percentage?
  - Attributed to the reduction of amorphous layer thickness

Tool	Energy (keV)	Increased activated percentage with respect to GSD200E2 (%)
Batch wafer implanter	15	N/A
Single wafer implanter	15	20.39
Single wafer implanter	12.45	10.66

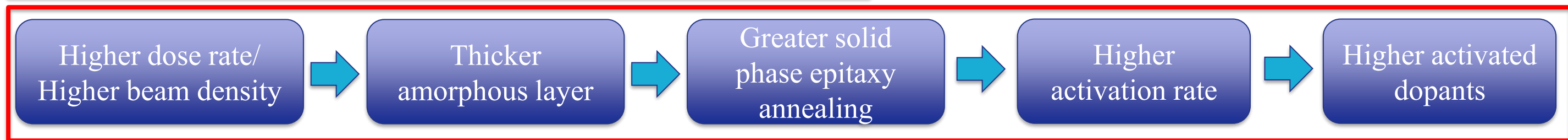
# Results and Discussion (product wafers)

## Rs analysis (annealed)



$$R_s = \frac{1}{\int_0^{x_j} q\mu N(x) dx}$$

- $R_s$  is the sheet resistance
- $\mu$  is the charge carrier mobility (holes)
- $N(x)$  is the net activated impurity concentration function of junction depth
- $X_j(x)$  is the junction depth
- $q$  is the charge carrier



# Summary

- A difference in beam current density between the single and batch wafer implanters led to a mismatch in electrical performance.
- In the past, several studies have been carried out to match performance, including:

Approaches	Limitations
Beam current reduction	Low throughput and increased beam instability
Beam size enlargement	Not applicable to spot beam implanters
Chiller temperature increment	Unable to standardize a single temperature across all products
Scan speed increment	Risk of wafer off-centering during implant and potential uniformity issues

- **In the present study, an energy trim factor of 83% (12.45 keV) was implemented at recipe level.**
  - Energy trim is not commonly used for device matching, but it can be considered when dose/dose trim is ineffective.
  - This enables flexible loading, allowing the same product to run on both implanters without added logistics and maintain high throughput.
  - Single wafer implanter demonstrates better stability
    - Productivity gain: ~ 5.3%
    - Down time reduction: ~ 1.8%

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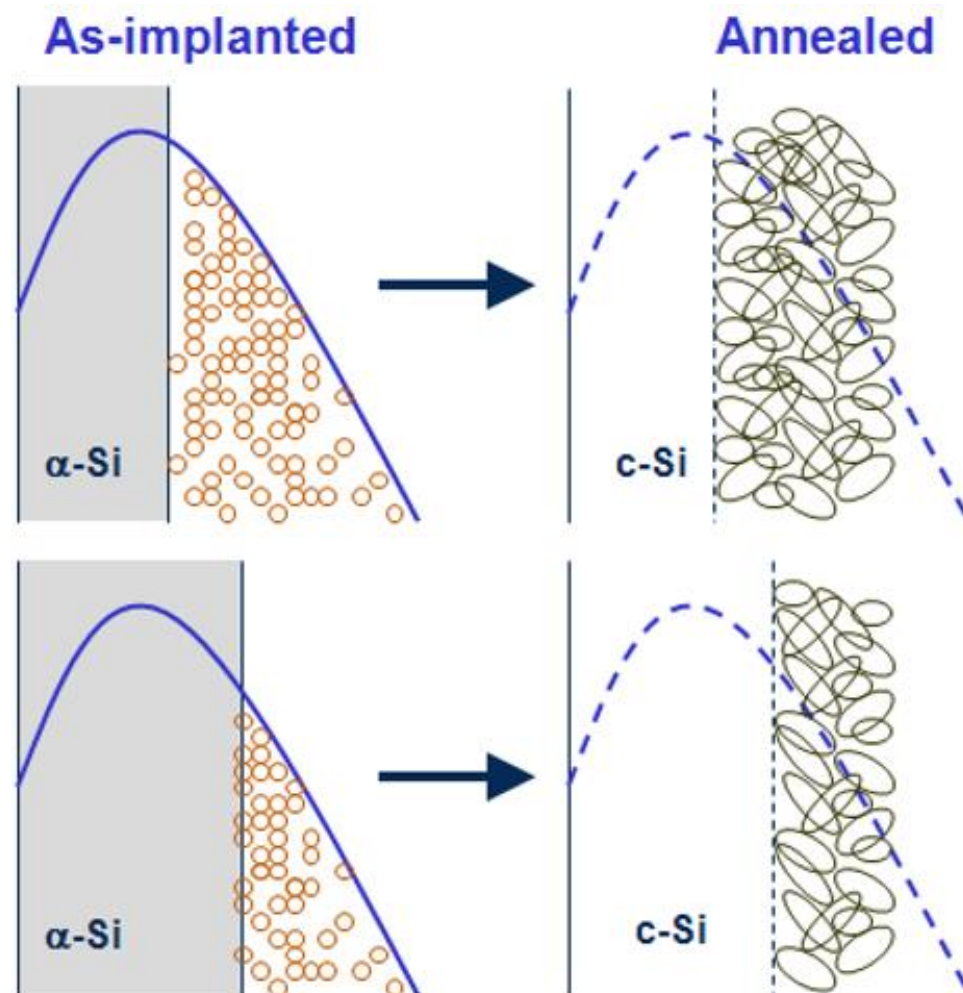
**THANK YOU !**

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# APPENDIX

# Impact of amorphous thickness on dopant activation and clustering (Theory only)



- Thicker amorphous layer
  - Improved electrical activation
  - Fewer residual defects
    - Greater solid phase epitaxy annealing ( $E_a = \sim 2.3 \text{ eV}$ ) vs standard annealing to get rid of defects and get dopant into substitutional site ( $E_a = \sim 5 \text{ eV}$ )
    - Better activation rate

**What is solid phase epitaxy?**  
 Regrowth of crystal from amorphous region using underlying substrate as the template

# Results and Discussion (test wafers)

## Rs (annealed)

Tool Type	Beam current (mA)	Beam density (mA/m <sup>2</sup> )	Rs Mean (Ohm/sq)	Std Dev (%)	Processing time (s)
Batch wafer implanter	6	~ 9	118.87	0.60	~ 1518
Single wafer implanter	0.6	~ 8	119.14	0.46	~ 1553
Single wafer implanter	6	~ 78	112.00	0.44	~ 162

- At 6 mA, the Rs for single wafer implanter is approximately 6 ohm/sq lower than the batch wafer implanter
- Rs was matched (within 1 sigma) under comparable beam densities by lowering the beam current of the single-wafer implanter to 0.6 mA
- Single wafer implanter with uniform scanned beam improved the Rs uniformity by around 0.15%.

Reducing the beam current to a comparable level of beam density matches the sheet resistance performance



Reducing the beam current to a comparable level of beam density results in 90% throughput loss



Undesirable



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