Damage control of ion implantation for advanced doping process by using in-situ temperature control

KyungWon Lee[1, 2], Michael Saied Ameen[2], Leonard Michael Rubin[2], Dwight Dongwan Roh[2], Rimpyo Hong[2], Ronald Norman Reece[2], DaeHo Yoon[1*]

[1]Sungkyunkwan University, 2066, Seobu-ro, Jangan-gu, Suwon-si, Gyeonggi-do, 16419, Republic of Korea

[2]Axcelis Technologies, Inc., 108 Cherry Hill Dr. Beverly, MA, 01915, U.S.A.

[*]E-mail address of the corresponding author: dhyoon@skku.edu

Abstract

Most silicon nano-devices use ion implantation doping for electric characteristics due to precise control of concentration and location of the dopants. A consequence of ion implantation is the damage to the silicon caused when injecting dopants into silicon substrate that break the silicon structure. This damage causes leakage or electron trapping in device circuits. Therefore, minimizing implant damage is of high importance. In general, ion implantation uses photoresist coatings, which can endure no more than 200 °C to make selected area doping. We characterized ion implantation damage on bare wafers by optimizing the process temperature during implant. Elevated temperatures during implant induce "self-annealing" which reduces the damage to the silicon structure as the implant occurs. We propose that *in-situ* temperature control can limit ion implant damage on the transistor well and photo diode steps on advanced Complementary Metal-Oxide Semiconductor (CMOS) image sensor devices.

Keywords: Ion implantation, Implant damage, Implant defect, Shallow junction

1. Introduction

Ion implantation is used in advanced CMOS devices because it allows precise control of the dopant depth and concentration. **Error! Reference source not found.** However, since the ion is forcibly injected into the silicon substrate, implant damage to the silicon lattice occurs **Error! Reference source not found.**, **Error! Reference source not found.** This implant damage could be eliminated in the subsequent heat treatment process, but due to the constraints of other processes, annealing temperature is limited and is not sufficient to relax the implant damage **Error! Reference source not found.**. Damage control is required because residual defects are sources of leakage current or degraded electrical characteristics **Error! Reference source not found.**,**Error! Reference source not found.**. In general, ion implantation requires the use of photoresist resins to make selected area doping. These materials are temperature sensitive and can only withstand temperatures up to about 200°C. We used a wafer temperature during implant between 150°C and 200 °C in this experiment to study damage control in a regime that is compatible with photoresist technologies.

2. Experiment

In this experiment, we used an Axcelis Technologies Purion H™, high current ion implant system. In the ion implanter, the ionized dopants are extracted through an arc slit and electrode assembly [7]. The ion then enters the beamline and only ions of the correct charge/mass ratio are properly steered by the Atomic Mass Unit (AMU) magnet. The resulting monoenergetic beam is then focused and scanned over the wafer.

To carry out the normal ion implantation process at room temperature, the wafer is cooled by circulating cooling water in the backside of the ESC (electro-static chuck) and flowing N_2 gas through small holes in the surface of ESC to increase thermal conductivity [8]. For in-situ temperature control, a 2 zone heater is located at the back of the ESC, shown in Figure 1 (a). The location of the ESC in the endstation is shown in Figure 1 (b). The in-situ temperature profile for several wafers are shown in Figure 1 (c). The wafers undergo a preheat process to keep the wafer temperature constant. The preheat takes about 10 seconds. The total temperature range across several wafers is less than +/-2.5°C after temperature stabilization.

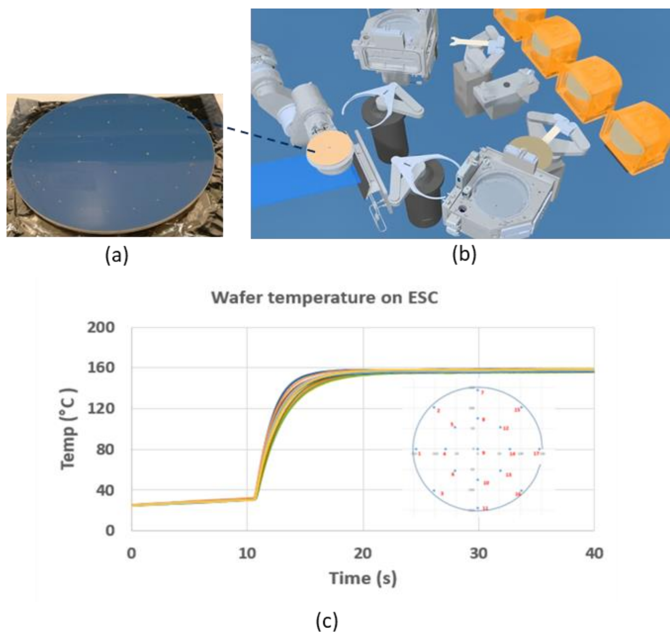

Figure 1 (a) Heated ESC (b) Wafer handling end-station (c) 17points of wafer temperature profiles on ESC across several wafers

The change in damage with implant temperature was measured using ThermaWave (TW). TW is a relative measurement value indicating the degree of damage of the silicon lattice **Error!**

Reference source not found.. The change of implant damage by beam current was measured by TW at room temperature and 150°C. In addition, the sheet resistance (Rs) was measured by the 4-point probe method to determine changes in implant damage versus beam current at room temperature and 150°C [10]. After ion implantation, the annealed samples were analyzed using cross-section Transmission Electron Microscopy (TEM) to compare defects at room temperature and 150°C. The damage difference on prefabricated fin structures as a function of temperature was measured with TEM.

3. Results and discussion

The difference of TW value was used to estimate damage differences. The ion implant condition is phosphorus, 10 keV, 2.5x10^{15} atoms/cm^2. As the temperature increases, the TW value decreases linearly, as shown in Figure 2.

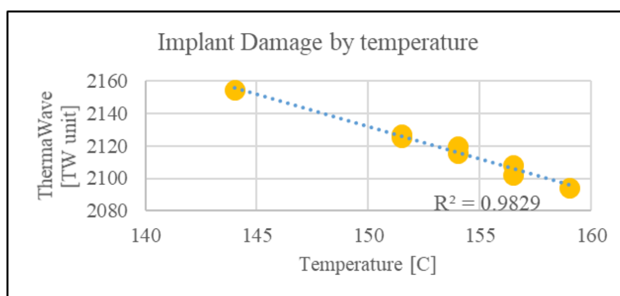

Figure 2 TW value versus temperature for phosphorus, 10 keV, 2.5x10^{15} atoms/cm^2 on as-implanted (un-annealed) samples

Formatted: Left

The damage difference from varying the ion beam density (beam current) was measured using TW. Beam current is not related to TW uniformity because the standard deviation was 0.32% at 18°C and 0.20% at 150°C. On the other hand, the average TW value at 150°C is 9.3% lower

than at 18°C as shown in Figure 3(a). This indicates temperature is a main factor in implant damage. In general, since most of the dopant is not activated immediately after the ion implantation, the sheet resistance has a high value [12]. Comparing the sheet resistance values, the 150°C implant has a 72% lower Rs value than at 18°C; see Figure 3(b). The reason why the Rs is lower at 150 °C is that the self-annealing effect of the process enhances the regrowth of the silicon lattice and more of the ions are activated **Error! Reference source not found.**.

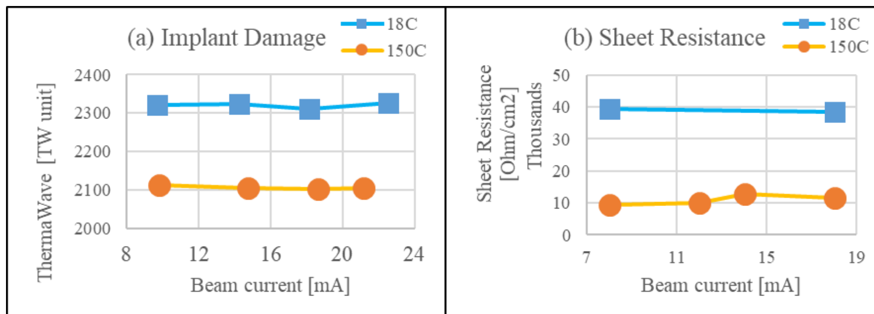

Figure 3 Effect of implant temperature and ion beam current for phosphorus, 10 keV, $2.5x10^{15}$ atoms/cm^2 (a) Ion implant damage comparison and (b) activation comparison using sheet resistivity for as-implanted (un-annealed) samples.

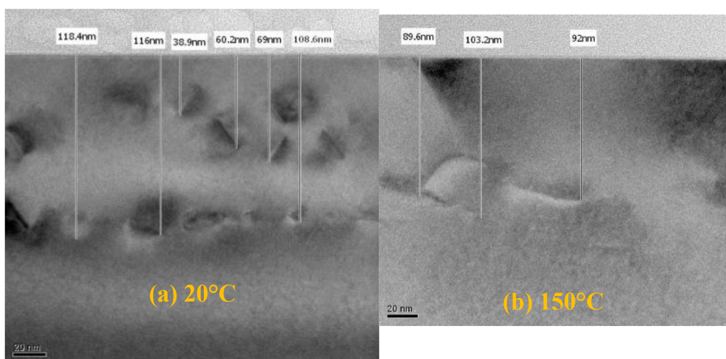

Figure 4: Cross section TEM images of arsenic, 10 keV, $3x10^{15}$ atoms/cm^2 + arsenic, 60 keV, $8x10^{15}$ atoms/cm^2 after an anneal at 850 C for 45 sec N_2 100%. (a) Implant temperature 20°C (b) Implant temperature 150°C

TEM of implanted and annealed silicon is shown in Figure 4. The amorphization conditions were As, 10 keV, 3x10^{15} atoms/cm^2 and As 60 keV, and 8x10^{15} atoms/cm^2. Since the defects are not visible by TEM at temperatures above 1000°C, annealing conditions of 850°C, 45 sec in N_2 100% are used to observe defects **Error! Reference source not found.**. We observe that defects are generated at various depths in samples implanted at 20°C as shown in Figure 4 (a). On the other hand, for the TEM image of a 150°C implant shown in Figure 4 (b), the defect was observed only in the end-of-range region corresponding to As 60 keV. It was observed that the residual defect was significantly reduced in the sample using the *in-situ* temperature control of 150 °C.

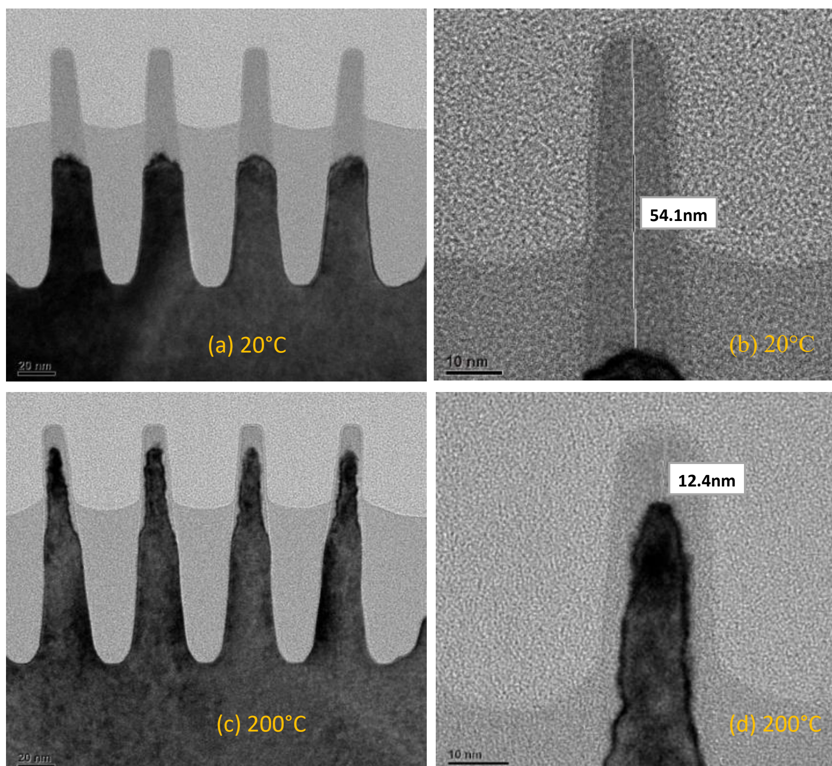

Figure 5 TEM ~~data~~ image of phosphorus, 10 keV, 5x10^{14} atoms/cm^2 (as-implanted) on fin structures. (a.b) Implant temperature 20° C, (c,d) Implant temperature 200° C.

After ion implantation into a fin structure similar to a real device, TEM images were compared. In the fin structure, the black area is crystalline silicon and the gray area is amorphized silicon. In the sample implanted at 20°C as shown in Figure 5 (a), it is seen that all of the regions higher than the middle of the fin are amorphized. However, in the sample implanted at 200°C as shown in Figure 5 (b), only the outer part of the fin structure was amorphized. This suggests that it will be easy to be re-crystalized with a subsequent heat treatment process **Error! Reference source not found.**.

4. Conclusions

Warm implant with *in-situ* temperature control is effective in reducing implant damage. It is considered that there is a curing effect by self-annealing as evidenced by sheet resistance. TEM images show that the defects of a wafer after implant at a temperature higher than room temperature are reduced. The potential applications of this damage control method will be adopted on advanced CMOS and CIS device at junction area of CMOS [17] or photo diode area of CIS [18].

Acknowledgments

The authors would like to thank the technical team of Axcelis Technologies, Inc. ATC (Advanced Technology Center) to evaluate characteristic of the in-situ implant temperature control experiments.

Funding

This research did not receive any specific grant from funding agencies in the public, commercial, or not-for-profit sectors.

References

[1] Mayer, James W. "Ion implantation in semiconductors." *1973 International Electron Devices Meeting*. IEEE, (1973): pp. 3-5.

[2] Morehead, F. F., et al., "Formation of amorphous silicon by ion bombardment as a function of ion, temperature, and dose." *Journal of Applied Physics* 43.3 (1972): pp. 1112-1118.

[3] Mok Kai Rine, et al., "*Modelling and simulation of ion implantation induced damage*." Diss. (2007).

[4] Gibbons, James F. "Ion implantation in semiconductors - Part II: Damage production and annealing." *Proceedings of the IEEE* 60.9 (1972): pp. 1062-1096.

[5] Pipes, Leonard C., et al., "NMOS source-drain extension ion implantation into heated substrates." *2014 20th International Conference on Ion Implantation Technology (IIT)*. IEEE, (2014): pp. 1-6.

[6] Wood, Bingxi Sun, et al. "Fin doping by hot implant for 14nm FinFET technology and beyond." *ECS Transactions* 58.9 (2013): pp. 249-256.

[7] Ian G. Brown, *The physics and technology of ion sources*. John Wiley & Sons. (2004): p. 61-86.

[8] Asano, Kazutoshi, et al. "Fundamental study of an electrostatic chuck for silicon wafer handling." *IEEE Transactions on Industry Applications* 38.3 (2002): pp. 840-845.

[9] Dortu, Fabian. *Low-frequency modulated optical reflectance for the one-dimensional characterization of ultra-shallow junctions*. Diss. Ph. D. thesis, Katholieke Universiteit Leuven, (2009).

[10] Smits, F. M. "Measurement of sheet resistivities with the four-point probe." *Bell System Technical Journal* 37.3

(1958): pp. 711-718.

[11] Hickey, D. P., et al. "Cross-sectional transmission electron microscopy method and studies of implant damage in single crystal diamond." *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* 24.4 (2006): pp. 1302-1307.

[12] Wolf, S., et al. *Silicon processing for the VLSI era, Volume 1-Process technologies.* (1986): pp. 393-398.

[13] Cembali, G. F., et al. "Self-annealing of ion-implanted silicon: First experimental results." *Applied Physics Letters* 38.10 (1981): pp. 808-810.

[14] Borisenko, Victor E., et al. *Rapid thermal processing of semiconductors*. Springer Science & Business Media, 2013.

[15] Camillo-Castillo, et al. "Impact of dopant profiles on the end of range defects for low energy germanium preamorphized silicon." *Materials Science and Engineering: B* 114 (2004): pp. 312-317.

[16] Tsai, M. Y., et al. "Recrystallization of implanted amorphous silicon layers. I. Electrical properties of silicon implanted with BF+ 2 or Si++ B+." *Journal of Applied Physics* 50.1 (1979): 183-187.

[17] Miyashita, T., et al. "Feasibility Study of Solid-phase Epitaxial Regrowth (SPER) as an Ultra-shallow Junction (USJ) Technology for High-performance CMOS Devices." *2006 International Workshop on Junction Technology*. IEEE (2006): pp. 92-95.

[18] Goiffon, Vincent, et al. "Radiation damages in CMOS image sensors: testing and hardening challenges brought by deep sub-micrometer CIS processes." *Sensors, Systems, and Next-Generation Satellites XIV*. Vol. 7826. International Society for Optics and Photonics, (2010).