

Contamination Control in Axcelis Purion Platform Ion Implanters

David A. Kirkwood, James Deluca, Jonathan David
Axcelis Technologies Inc.,
Beverly, MA

Abstract— Industry consolidation in semiconductor manufacturing, driven by commoditization and decreasing margins, is placing ever increasing pressure on fab productivity. Concomitant technology innovation, shrinking device geometries, the transition to non-planar transistors and novel device structures (such as CIS or IGBT) make yield attainment increasingly challenging. The defect level performance of semiconductor manufacturing equipment, in particular in ion implantation, is one of the critical parameters contributing to overall yield performance. This is evidenced through recent large shifts in both particle and metals requirements from device manufacturers. Traditional implanter design approaches, focused on glitch reduction or beam current modulation, are necessary but insufficient to attain simultaneous compliance of availability, throughput and defect levels.

In this paper, a holistic approach to defect control is detailed. Examples of contamination control best practices are described. These are combined into an overarching design for process cleanliness (DfPC) methodology, through identification and mitigation of defect opportunities (particulates, metals). Data from the Purion platform of ion implanters demonstrate that, through application of an integrated, common design method, required defect performance can be attained across multiple ion implant platforms.

Keywords—particles; metals; yield; productivity

I. INTRODUCTION

The semiconductor manufacturing ecosystem has witnessed a sustained period of consolidation, driven by the increasing commoditization of end products in the consumer electronics market and the increasing challenges in R&D as many conventional approaches to scaling reach the end of their usable life [1]. As such, traditional boundaries between Logic and Memory manufacturing are disappearing, with most of the major industrial actors participating in both sectors, whether in adopting a Foundry model such as TSMC and GF, or becoming more vertically integrated such as Samsung.

The industrial dynamics mentioned above have had direct consequences for process flow in the manufacture of conventional CMOS technologies. Device yield and fab productivity are paramount concerns, and manufacturers are increasingly engaging with their upstream and downstream value chain partners to eliminate all potential sources of loss to either parameter. Historically, correlation between device yield and particulate excursions was not strong below a certain threshold of particle size, and most device failures had other

root causes [2], particularly in DRAM manufacturing where devices were less sensitive to surface contamination. Furthermore, many process steps were followed by PR removal or cleaning steps, the result of which meant that device yield was not sensitive to the cleanliness state of the preceding process step.

Several paradigms in the industry have however acted in concert to change this mode of thinking. Shrinking device geometries; new device types (non-planar CMOS; CIS); changes in Fab type and utilization, have all acted to heighten the sensitivity of process yield to particulate levels. This may be seen through an examination of the particulate specifications of device manufacturers to their equipment suppliers. Figure 1 depicts particulate UCL's from several sample device manufacturers. These control limits are specified as an absolute limit on the number of adders, and the smallest particle size from which these numbers will be integrated. Whilst many manufacturers do still specify average particle performance, this is not meaningful since particle generation follows lognormal statistics [4].

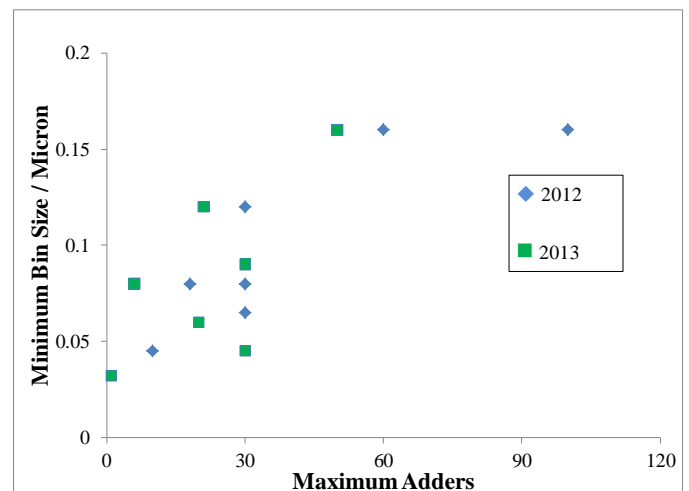


Figure 1: Particle Specification Evolution

Despite the requirement to anonymize the data, it may still be seen that within 1 year the limit on the absolute number of defects per process step is being reduced by 50% or more, and the smallest particle size that is being measured is being reduced concomitantly in most instances. The latter has in general always been true – as device features shrink, so too does the minimum “killer defect” size. For each device generation the smallest particle measured has been reduced by

a factor of $\sim 1/(2)^{1/2}$, however recently this has accelerated, both in the magnitude of the change in minimum bin size and the rate at which this has dropped. Within one year one foundry dropped from 90nm to 45nm measurements within the same device generation.

One reason for the latter discontinuity in change is the challenge faced by most industrial actors in attaining the required yield levels when transitioning from planar to non-planar device geometries. It is anticipated that the material modification steps in particular have an increased sensitivity to particulate defect levels relative to older planar device geometries. As such, many device manufacturers have sought to engage with their value chain partners in order to drive down defect levels.

II. THEORY - SOURCES OF PARTICLES IN ION IMPLANTATION

The contamination level requirements of semiconductor processing impose stringent constraints on the production equipment used in the wafer process environment. In the ion implanter, particularly in the beamline, exposure to direct beam strike, large temperature and pressure gradients generate the opportunity for material disintegration, potentially leading to the loss of process integrity and excessive contamination [5]. Beam assisted transport mechanisms from material surfaces are also considered contributors to particle accumulation.

The continual reduction in lower bin size places a particular burden on ion implantation. The distribution of particles generated in implant is not linear, but rather increases as particle size diminishes. This challenge also extends to the metrology equipment manufacturers – at the smallest particle sizes *in situ* measurement is no longer viable, and offline measurement is slow and subject to uncertainty based on the quality of the starting substrate.

The section below lists six of the primary means by which particles may be generated by, or introduced into, the ion implanter. Appropriate design of parts for the beamline and end station, not only in terms of material composition but also in terms of manufacturability, serviceability etc. all play a pivotal role in mitigating components' potential to generate particles. This list is generated from a basic Ishikawa analysis of the root causes to the generic problem of particulates in ion implantation.

- **Beam generated.** It is not possible to prevent beam strike on some of the implanter components during ion implantation in normal operation. At high energy and current, this results in either sputtering or ion beam milling. Grazing angle incidence interactions can then either impart momentum to surfaces particulates or lift surface material via the beam potential. Other beam-induced processes which can occur include delamination of surface layers
- **Gas-borne.** Every gas feed into the system is capable of introducing particles. These include dopant gas source feed material, beamline gas bleed, plasma flood systems, venting lines etc. In addition, materials can backstream in roughing lines back into the main pumping system without careful vacuum design.

Vacuum leaks, normally arising after PM or hardware change, are common causes of particle level elevation

- **Electrical Discharge.** HV electrodes, essential for beam transport, are employed throughout the vacuum system, and incorrectly designed stand-offs or incorrect material selection may result in discharges which subsequently generate particles [6]. Electrical discharge in the post analysis region, especially in the vicinity of the wafer, can yield very high excursion levels ($>1E5$), and often occurs at a voltage far below the theoretical levels, due to a combination of surface material instigating the arc and the presence of the beam plasma reducing the effective potential barrier to discharge ignition. ESD in wafer handling components can also arise, which typically produces intense “cluster” signatures. In the source region, pushing source parameters towards the end of source life usually results in a degradation in extraction electrode stability, thus resulting in particle generation.
- **Cross contamination.** This may come from a number of sources, however the end result is that a component of the tool transfers material to the wafer which does not itself originate from that component. This is frequently observed with back sputtered material onto wafer handling components, or from material transferred from wafers in the vacuum system, and is one route by which metals may be transferred to the wafer surface. The formation of multiple thin layers of dopant material and subsequent stress induced delamination has been observed.
- **Mechanically generated.** Ion implanters rely on moving parts in vacuum to either tune the ion beam or move the wafer. Contact with the wafer should always be minimized as this is a direct route for particle transfer, as should all motion above the wafer plane. Frictional interference will also result in particle generation
- **Foreign contaminants.** Any activity which introduces material into the tool, normally during preventative maintenance (PM), has the potential to generate or introduce contamination. *In situ* cleaning can result in material introduction to the tool (residue from deposits, wipe fragments, alkali metals from sweat). Third party consumable components, with surface finish not matching OEM specifications, have also been historically linked to field particle issues

The above lists the generic opportunities for defect introduction to the process flow from ion implantation. Traditionally, ion implantation has been segmented into high energy, medium current and high current. Particulates have largely been of lower concern to the former two implanter types, and when observed are generally a result of mechanical mishandling or valve issues in the end station, or, rarely, ESD arising from loss of charge control. Typically this is reflected in the lower PM frequency of these systems.

III. APPROACH TO CONTAMINATION IN PURION IMPLANTERS

Designing in particle mitigation solutions for contamination control is well understood and in deployment in most ion implanters. For example, all Axcelis high current ion implanters have utilized high voltage shields which detect the early onset of arc formation and act to interrupt the HV supplies to allow the arc to dissipate before high levels of particles can be generated. However, in order to meet the aggressive specifications being demanded by device manufacturers in terms of reduced levels, it is necessary to exceed these minimum requirements.

Conventional mitigation techniques using process control, such as detuning the source, are in general inimical to optimal productivity. In production, the primary driver of defect performance is normally the quality and frequency of PM. This is also largely out of the direct control of manufacturers, and is often the result of a combination of second sourcing unapproved materials by the device manufacturer from local, cheaper vendors, and from poorly performed maintenance procedures inside the vacuum system.

The Axcelis Purion platform of ion implanters has utilized a methodology called Design for Process Cleanliness in order to enable the scaling of novel device geometries at the required yield. The key principle is that of simultaneous compliance, which necessitates that the implanter must meet particle spec for all implant energies and doses, and not just a narrowly defined monitor recipe. This places a number of constraints on the designer, particularly for optimum transport of high current ion beams. This holistic approach moves beyond the component level considerations described in the preceding section, and includes the following detailed below:

- **Design for Serviceability.** In order to remove opportunities for defect introduction to the system, all Purion ion implanters are designed such that all invasive PM procedures may be undertaken remotely from the tool. The removal of *in situ* cleaning activities is critical to ensuring defect performance in production. This is achieved via a modular design approach whereby each critical optical element of the beamline, and the process chamber, is lined in such a manner that it can be readily removed from the system and swapped out. The concomitant reduction in downtime is also a primary consideration, thereby enhancing productivity.
- **Five filter design.** For high current applications, the Purion H implanter is designed around the concept of five primary filters that act to suppress the transport of particles by the ion beam. In general, there are two primary modes by which particles may be transported around the implanter vacuum system – beam assisted and turbulent flow. The former is a consequence of high beam potential, particularly at high current and low energy, which results in the entrainment of particles which acquire negative surface charge. It has been demonstrated elsewhere that potential barriers will act to impede transport of these particles in the beam, however any lens element designed specifically for this purpose will also act to perturb the ion beam transport itself. In the Purion platform, the optical design of the

final energy filter lens element, which is the most critical for governing the particle performance of the system, is designed such that the particle suppression and beam optical elements act in concert, with particle suppression lens elements which minimally perturb the beam.

- **Guaranteed Alignment.** Variability in ion beam trajectory is one of the primary sources of particulate level elevation on an ion implanter which is otherwise in good particle control. Through a patented mechanism the Purion platform is designed to eliminate motion of the ion beam as the ion source and extraction optics thermally cycle under different loads arising from the arc and extracted beam current. Downstream of the extraction, other critical optical elements are engineered such that the beam cannot be steered through system misalignment during preventative maintenance.
- **Leveraging the Implant Value Chain.** This strategic approach involves the upstream and downstream supply chain actors, and strategic partners, and includes working with materials suppliers and packaging providers to Fab integration teams, to move the particle focus from being tool specific to encompassing the entire value stream associated with semiconductor fabrication. For example, Axcelis patented graphite grade materials are designed to optimize particle performance and ease of PM whilst minimizing cost of ownership (CoO). Axcelis specify a double vitrification process on all HV electrode elements of the tool, that results in a smooth, particulate free surface that guarantees HV stability and uniformity of electric field. HV stability and particles have shown to directly correlate with graphite grade.

IV. DATA AND ANALYSIS

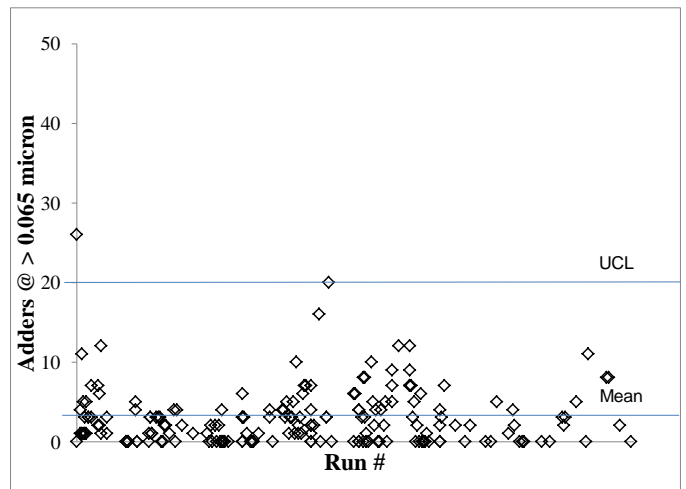


Figure 2: Purion M Field Data

In order to demonstrate the effectiveness of the design solutions detailed above, three independent sets of data are presented. The first example considers the Purion M system in a production environment. A common cause of particle excursions in other available medium current solutions is high

voltage breakdown in the final lens element, and the data presented demonstrate this is not the case for the Purion M. The second set of experiments were on a Purion H system in a controlled environment designed to test compliance to the particle specifications of a leading Logic manufacturer. Finally, a series of aggressive metals implants were conducted on all three implanters in the Purion suite of systems, to demonstrate efficacy of eradication of surface metal contamination.

Figure 2 depicts data taken over a 1 year period from the Purion M ion implanter at a customer site. The number of wafer starts per day was variable throughout the duration of the experiment. Measurements were made on bare Si and the sample frequency averaged 1 sample every other day (this represents a far higher sampling rate than would normally be conducted on a medium current tool in production). Historically, low tool utilization leads to particle excursions due to thermal cycling of the beamline components, however there were no data to support this occurring on the Purion M. The global mean was 3 adders at > 65nm, and compliance to the customer specified UCL was 96% throughout the duration of the evaluation. These data compare favorably to levels attained by the tool of record in production. Data were also taken at the lower 45nm bin size limit during the sample period, and were found to be equivalent to the >65nm data.

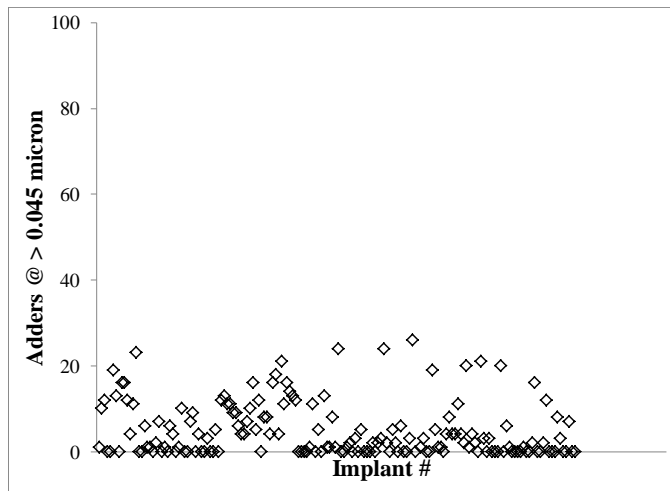


Figure 3: Purion H Lab Data

In Figure 3, data taken on the high current Purion H ion implanter is shown. All data were taken as 25 wafer lots with particle measurements on prime wafers with starting counts <100 @ >45nm. Particles were measured on a KLA-Tencor SP2 metrology system. The data were taken over a 1 week period during which the tool was running at 24x7 operation. The global mean was 4 adders at >45nm, with a compliance to < 20 adders at 94% and a compliance to < 10 adders for individual lots of > 90%. Recipes used were chosen to match current production requirements from a leading Logic Fab.

Finally, the metals performance of the Purion fleet was fingerprinted in order to verify the efficacy of the beamline filtering elements. The VPD ICP-MS data in Figure 4, which also contains the test implant conditions, demonstrate that the

metals levels for the implanter fleet exceed the requirements of even the most aggressive CIS manufacturing process flow.

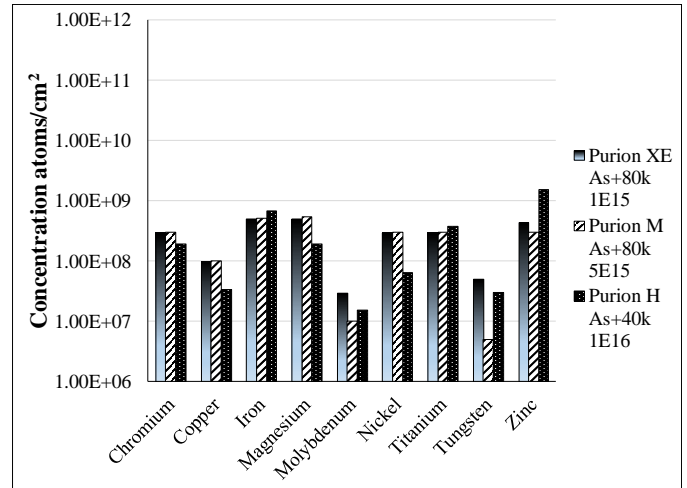


Figure 4: Purion VPD-ICMPS Metals Data

V. CONCLUDING REMARKS

The majority of leading CMOS fabrication processes now require defect levels of single digit adders at minimum particle sizes of >4xnm. Conventional approaches to particle mitigation in ion implantation do not suffice to meet these levels at the required rates of compliance. Furthermore, required metallic contamination levels are at or below the detection limit for certain devices. The DfPC methodology, applied to the Purion platform of ion implanters, enables the scaling of novel device geometries at the required yield. The beamline filtering elements allow both the Purion H high current implanter and the Purion XE high energy implanter to achieve similarly low metals contamination levels to the Purion M. All members of the Purion family of implanters are proven capable of consistently delivering metals contamination levels at or near the method detection limits.

ACKNOWLEDGMENT

The authors would like to thank YS Seo and other members of Axcelis Korea for obtaining data used within this work.

REFERENCES

- [1] R.R. Schaller, "Technological innovation in the semiconductor industry: a case study of the International Technology Roadmap for Semiconductors (ITRS)", Doctoral Thesis, George Mason University, 2004
- [2] A. Vanderpool and B. Whitson, Symposium of Semiconductor Manufacturing, IEEE (2003), p505
- [3] A. J. Strojwas "Tutorial on Design for Manufacturability for Physical Design", PDF Solutions Inc., 2005
- [4] F. Sinclair, J. Blake and S. Brubaker "Lognormal statistics for particles: models, causes and implications", Proceedings of the International Conference on Ion Implantation Technology, 1998, 207
- [5] M.E. Mack, G.C. Angel, M.L. Pascucci, D. Prisky, NIMPRB 96, (1995), 80-86
- [6] Vanderberg, B.H., Perel, A.S., Horsky, T.N Proceedings of the International Conference on Ion Implantation Technology, 1998, 207