Study of Controlled Oxygen Diffusion Approaches for Advanced Photoresist Strip

Shijian Luo[1, a], Orlando Escorcia[1], David Mattson[1], Carlo Waldfried[1], Dongwan Roh[1], and Ivan Berry III[1]

[1]Axcelis Technologies, Inc., Beverly, MA 01915, USA

[a]Shijian.Luo@axcelis.com

Keywords: HDI strip, residue removal, substrate loss, metal oxidation, dopant retention.

Abstract. Two alternative plasma strip processes were developed to meet the photoresist (PR) removal requirements of future technology nodes. Compared to traditional oxidizing chemistries, the new plasma strip approaches showed significantly lower silicon oxidation and substrate loss, while achieving good residue removal capabilities. Plasma strip-induced dopant loss and profile changes were also evaluated for gate-first and gate-last high-k/metal gate applications.

Introduction

The applications of high dose implant (HDI), ultra shallow junction (USJ) implants and high-k/metal (HKMG) gate stacks pose challenges to the existing PR strip technologies. The resist removal techniques used for HDI resist strip on USJs are required to minimize substrate oxidation and damage, and prevent the loss, redistribution and deactivation of implanted species, while efficiently removing the carbonized crust and completely cleaning PR and residues [1]. The strip and clean process must also preserve critical dimensions of the gate and sidewall spacer materials. HKMG stacks add additional constraints such as: galvanic corrosion [2], threshold voltage (V_T) control and stability [3], and oxidation of the interfacial layer under the high-k dielectric [4,5].

The traditional plasma ashing approaches all have some limits which inhibit their ability to meet the advanced strip requirements. Fluorine-containing chemistries are very effective for crust breakthrough and residue removal, but are known to produce substrate damage and dopant bleaching. Oxidizing chemistries (O_2/N_2:H_2) cause high substrate oxidation. Forming gas (96% N_2+ 4% H_2) by itself (without added oxygen) can achieve low substrate oxidation, but has poor crust and residue removal capability and has been shown to cause issues with dopant retention and activation [6-8].

In order to overcome all these limits, two non-oxidizing strip approaches were studied and compared with traditional solutions. Silicon and metals oxidation, substrate loss, dopant retention, as well as resist and residue removal capability have been evaluated.

Experimental

All work in this paper was done on a 300mm, three-module, six-chamber Axcelis Integra dry-strip system. SEM analysis was utilized to evaluate post-strip cleanliness and residue removal capability of strip processes. Spectral ellipsometry, TEM and XPS were used to measure substrate damage and oxidation. Metal (TiN) oxidation was also monitored by measuring pre- and post-strip sheet resistance (Rs) on blanket films. Post-strip dopant loss and profile changes were evaluated using SIMS. Rs measurements were also employed to determine dopant retention.

Results and discussions

In this study, two new non-oxidizing chemistries (C-1 and C-2) have been evaluated for their HKMG compatibility while minimizing substrate loss and removing HDI residues efficiently. Table 1 summarizes the performance results of the approaches of two new chemistries, as well as acid clean, traditional oxygen + 10% Forming Gas (O_2+FG) and pure Forming Gas (FG) chemistries.

The hot acid clean that is capable of removing HDI resist caused high SiN and SiGe loss. (The TiN ΔRs was not measured due to high TiN etch rate). Among the dry strip approaches, O_2/FG had the highest ash rate, but also the highest substrate (Si, SiN, SiGe) loss and metal (TiN) oxidation. FG showed low substrate loss, but changed the TiN sheet resistance (Rs), had low ash rate, and was less effective at residue removal capability for some HDI strip levels. C-1 approach offered low substrate loss, good residue removal capability and relatively high ash rate, but less favorable metal oxidation results. This makes C-1 a good candidate for HDI strip and replacement gate HKMG but not gate-first HKMG cleaning applications where the metal gate edge is exposed to the plasma. C-2 exhibited low substrate loss, and the smallest change of TiN Rs, which is preferred over the negative Rs change produced by the FG process in most applications. C-2 also showed excellent HDI resist residue removal. XPS results of strip-plasma processed TiN wafers confirmed the results of the TiN Rs measurements.

Table 1 Performance of different strip approaches

Approach	AR (normalized to FG only)	Total Si Loss (Å after 20 passes)	Total SiN Loss (Å after 5 passes)	Total SiGe Loss (Å after 20 passes)	Metals (TiN) Oxidation, measured by ΔRs (%)	Residue Removal
C-1	4.0	4.8		2.5	47	Good
C-2	1.0	3.8	0.14	2.53	0	Excellent
O_2/FG	7.8	10.4	1.4	15.5	45	Fair
FG	1.0	4.0	0.13	2.7	-10	Fair
Acid clean			7.8	34.5		Good

Several levels of HDI wafers were tested with C-1 and C-2, both of which demonstrated very good PR cleaning and residue removal efficiencies. Fig. 1 shows one application of HDI strip for post LDD (lightly doped drain), in which the structured wafers were processed with FG-only and C-2 approaches. The post-strip SEM images show that the wafer treated with C-2 is completely clean, while FG-only still has residues.

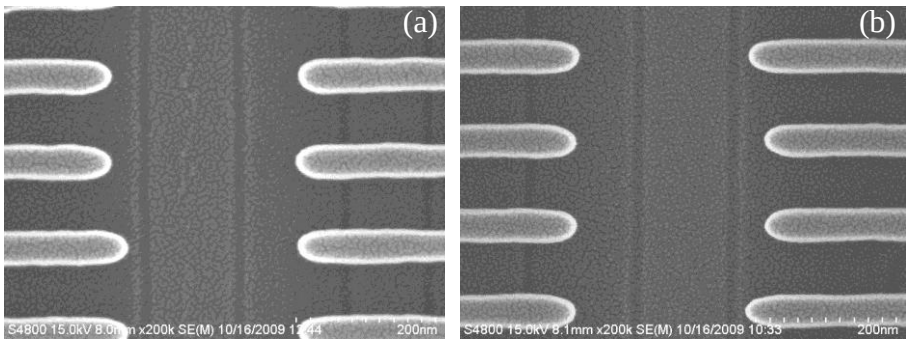

Fig. 1 Post-strip SEM images of HDIS for post LDD: (a) FG-only, (b) C-2.

For high-K/metal gate stack strip, the traditional oxidizing chemistries also can affect the interfacial oxide between the high-k and the silicon. Diffusion of oxygen through the high-k material leads to a birds-beak under the high-k layer, as illustrated in Fig. 2. This birds-beak results in effctive oxide thickness (EOT) variations and possibly strain-induced gate leakage. The height of this birds-beak was characterized for O_2/FG, FG-only and C-2 for a HfSiON high-k and was found to be ~4Å, 0Å, and 0Å respesctively. It was reported by Brunet, et. al. [3] that oxygen diffusion through HfO_2, and HfZrO is much higher than for HfSiON, so for these other high-k materials the extent of the birds-beak may be greater.

In an application of post-extension implant strip over exposed high-k/metal gate, FG-only, C-1 and C-2 approaches were explored with integrated product test wafers from a logic chip manufacturer. Both FG-only and C-2 showed clean results with no residues. A very small amount of

residues was found with C-1. However, these residues were removed with room temperature DI water rinse. Post strip wafer inspection showed zero defects for FG-only and C-2 processes. C-2 also showed the lowest TiN loss. The test structure after 7x plasma exposure to the C-2 dry strip process showed no difference in substrate dimensions, and undetectable metal gate loss and Si recess, compared to a control sample without plasma exposure.

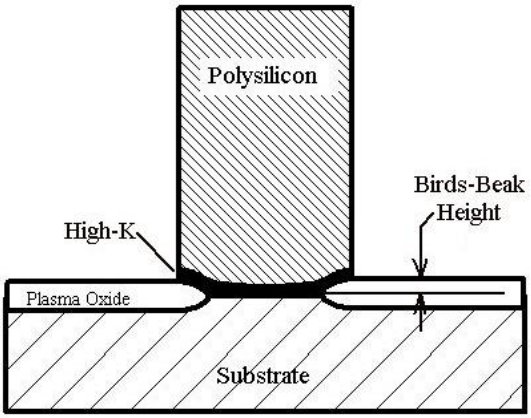

Fig. 2 Interfacial oxide growth at gate-edge using oxidizing plasmas.

In addition to residue removal capability and low substrate loss, HDIS strip solutions also must preserve the electrical characteristics of the device, which are related to dopant retention, dopant activation and dopant distribution. In one application, Si wafers were treated with source/drain extension and halo implants with a Xenon pre-amorphization (Xe^+, C^+, BF_2^+, As^+), then plasma stripped, annealed, and eventually analyzed using SIMS and Rs measurements. SIMS depth profiles of As, B and O are shown in Fig. 3. All three strip processes showed little Rs shift. Compared to the control (no strip process), the C-2 process had the smallest profile change for As. The B profiles were slightly different from each other in the near-surface region. The O_2/FG plasma process had the highest surface oxidation, which resulted in a shift in the As profile. C-1 and C-2 had little surface oxidation, and little As profile change. Estimated metallurgical junction depth (Xj) for As and B were very close for all three strip approaches, considering the much higher surface oxidation with O_2/FG strip.

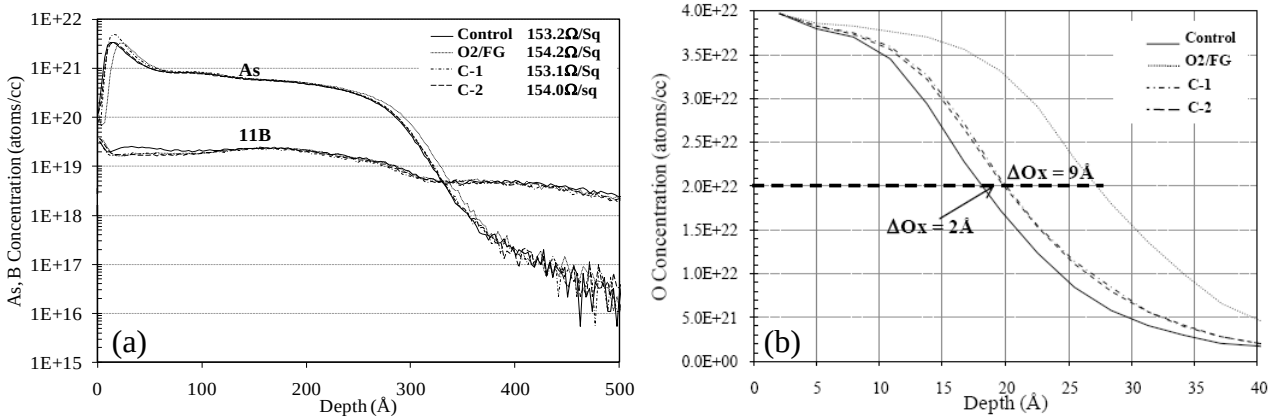

Fig. 3 SIMS depth profiles: (a) As and B, (b) O.

Besides the substrate damage induced during plasma strip processes, post-strip substrate oxidation must also be reduced. Fig. 4 demonstrates that a loadlock on Axcelis' Integra system with controlled wafer cooling in N_2 environment significantly reduced Si and metal (TiN) post-strip oxidation, compared to wafers cooled in air.

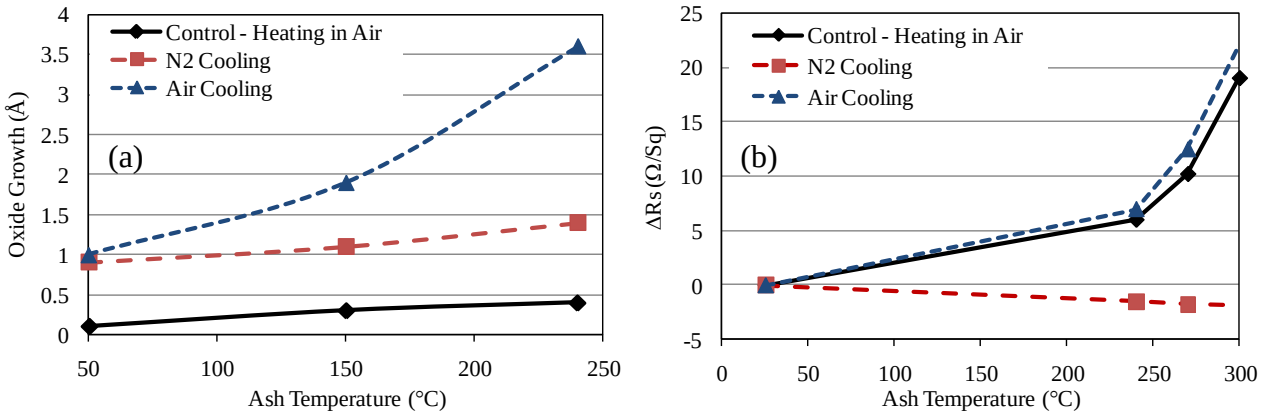

Fig. 4 Cooling environment effect of post FG-only strip substrate oxidation: (a) Si, (b) TiN.

It is speculated that hydrogen in the FG plasma creates vacancies in the silicon that are easily oxidized [7,9]. These hydrogen generated vacancies are well known [10] and can also explain hydrogen effects on arsenic transient enhanced diffusion [9].

Summary

Two controlled oxygen diffusion plasma strip approaches were investigated and developed for advanced strip such as HDIS and high-k/metal gate applications. Good residue removal capability, low Si and metal oxidation, low substrate loss, and good dopant retention were achieved simultaneously. Successful applications of these novel strip approaches on several customers' structure wafers have demonstrated a path to meeting the requirements of wafer cleaning of the 28nm technology node and beyond.

References

[1] F.Arnaud, H.Bernard, A.Beverina, R.El-Farhane, B.Duriez, K.Barla, D.Levy1: Solid State Phenomena, Vols 103-104, UCPSS 2004.

[2] S. Garaud, R. Vos, D Shamiryan, V. Paraschiv, P. Mertens, J. Fransaer, S. De Gendt: Solid State Phenomena, Vols 145-146, UCPSS 2008.

[3] L. Brunet, et. al: p. 29-30, IEEE Symposium on VLSI Technology, 2010.

[4] C. Hobbs, et. Al : 30.1.1, IEDM 2001.

[5] V. Narayanan, et. al: Appl. Phys. Lett., 81, 22, 2002.

[6] K. Han, S. Luo, P. Geissbühler, Q. Han, I. Berry, R. Sonnemans, V. Grimm and C. Krueger: ECS-ISTC 2007.

[7] K. Han, S. Luo, O. Escorcia, C. Waldfried, I. Berry: State Phenomena, Vols 145-146, UCPSS 2008.

[8] G. Mannaert, et.al: State Phenomena, Vols 145-146, UCPSS 2008.

[9] I. Berry, C. Waldfried, K. Han, S. Luo, R. Sonnemans, M. Ameen: IEEE Junction Technology, IWJT '08, 15-16 May 2008.

[10] M. Stavola: 5th Intl. Symp. On Advanced Sci. and Techn. of Silicon Materials (JSPS Si Symposium), Kona, Hi Nov10-14, 2008.