Study of Post Plasma Doping Photoresist Strip

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This paper reports on the study and development of post plasma doping photoresist (PR) strip processes which meet the requirements of good dopant retention and cleaning capability for this application. SIMS analysis of plasma implanted silicon wafers processed with these plasma strip approaches have shown improved dopant retention and profile in both n-type and p-type junctions. Stripping of implanted patterned PR wafers with these processes has revealed excellent cleaning and residue removal capability. This work demonstrates that these post plasma doped PR strip processes are viable candidates to meet the demanding clean requirements for USJ fabrication by plasma doping technology.

Introduction

The steady trend to smaller device nodes continuously requires reduction of ion implantation energy for shallower junctions and increase of implanted dose to maintain adequate sheet resistance (RS). For cost-of-ownership reasons, plasma doping technology has become an alternative to beam-line ion implantation in fabricating ultra-shallow junctions (USJ). Plasma doping is also attractive in replacing ion beam implantation for conformal doping of complex 3D structures, such as FinFET devices. However, one of the biggest issues with plasma doping of junctions is surface dopant retention. Up to 70% dopant losses during post plasma doped PR strip and cleaning have been reported (1). Like beam-line high dose implantation, plasma doping also forms a highly carbonized crust layer on top of the bulk resist, which renders the resist film much harder to break up and remove. Insufficient crust removal by most strip chemistries generates hardened residues on the substrate surface and leads to strip process defects (2, 3). Therefore, reducing dopant loss is critical in developing post plasma doping PR strip processes that also provide good cleaning capability. The conventional oxidizing strip chemistry ($O_2/N_2:H_2$) undercuts the crust easily and forms heavy residue, in addition to oxidizing the exposed materials and causing dopant loss. Forming gas-only ($N_2:H_2$) strip chemistry shows an unacceptably low removal rate to remove plasma doped resist and poor residue removal.

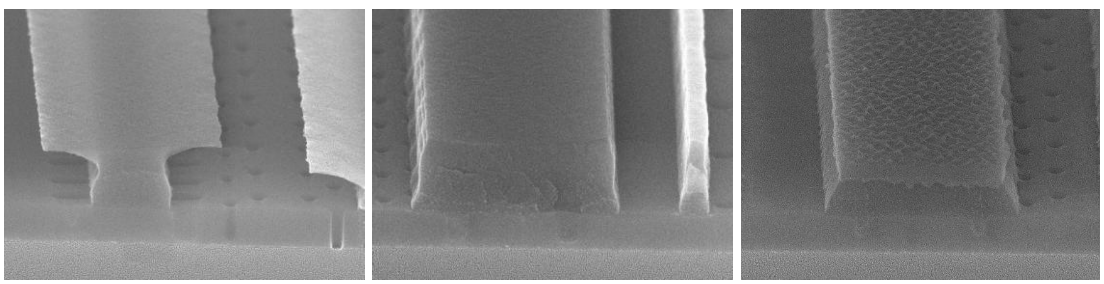
In this paper an Axcelis proprietary resist strip process was studied for plasma implanted PR strip. SIMS analysis and SEM cleanliness check of plasma doped wafers striped with processes of this chemistry demonstrated that these processes could provide good removal rate and low residue formation along with improved dopant retention. These processes have been successfully tested with integrated product test wafers.

Experimental

All studies in this work were carried out on a 300mm, three-module, six-chamber Axcelis Integra dry-strip system, with a microwave-driven, remote plasma source and a load-locked platform design which incorporates active wafer cooling. Patterned resist wafers and bare Si wafers (p-type and n-type) were plasma implanted at IBS on Pulsion® Plasma Immersion Ion Implanter with AsH_3, BF_3 and B_2H_6 plasma doping at different conditions accordingly. Wafers were then plasma stripped. SEM analysis was utilized to evaluate post-strip cleanliness and residue removal capability of strip processes. Plasma strip-induced dopant loss and profile changes were evaluated using PCOR-SIMS.

Results and Discussion

The first objective of this study was to clean the plasma implanted resist. A comparison test was done using three strip approaches, 2 conventional dry strip processes using $O_2/N_2:H_2$ and $N_2:H_2$ strip chemistries and an Axcelis proprietary process which will be called the AC process in the rest of the paper. The plasma doped resist samples were checked with SEM after 30 seconds partial strip. Figure 1 shows some of the SEM images.



(a) (b) (c)

Figure 1. SEM images of partially striped resist: (a) $O_2/N_2:H_2$, (b) $N_2:H_2$-only, (c) AC process.

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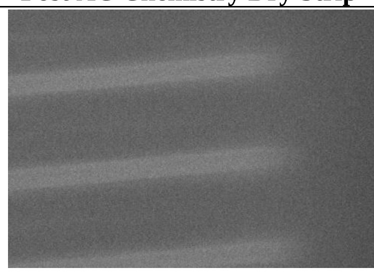
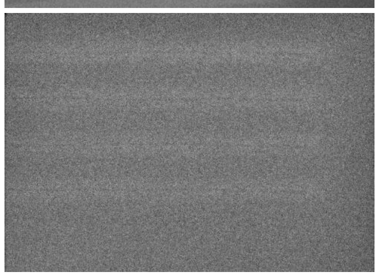
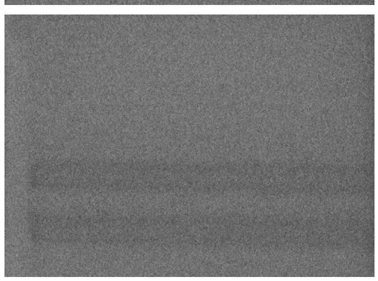
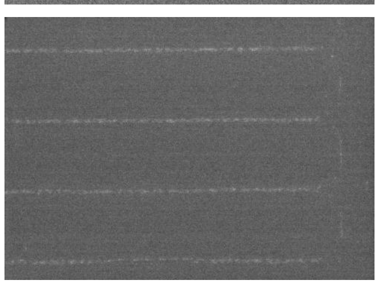
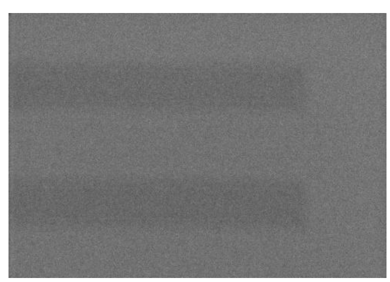
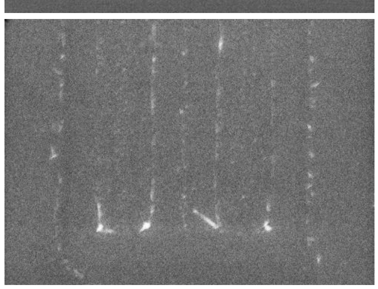
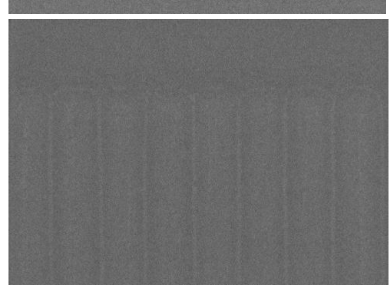
The oxidizing $O_2/N_2:H_2$ process showed poor selectivity of crust to bulk PR. The undercut of bulk resist left the crust overhang which would fall down on the wafer surface and form residues. The $N_2:H_2$-only had the slowest resist removal rate and was ineffective to cleaning the thicker features. The AC process demonstrated improved selectivity and similar removal rate as $O_2/N_2:H_2$ process without undercut.

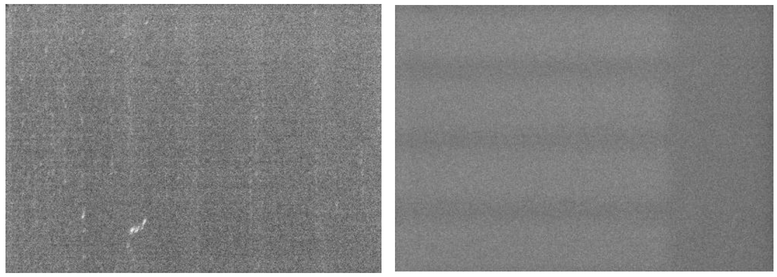
Patterned resist wafers implanted with eight different plasma doping conditions were investigated in this work, as shown in Table I. Different plasma doping conditions led to different changes of the resist layer, therefore the AC strip processes were optimized for each doping condition. SEM of the post AC strip samples showed that wafers of all eight implant conditions were either completely cleaned with no strip residue, or cleaned with a minor residue left which was easily removed by 30 seconds room temperature 500:1 dilute HF dip. SEM pictures of post strip samples in Figure 2 show only ghost images of implanted (open) and unimplanted (resist covered) areas.

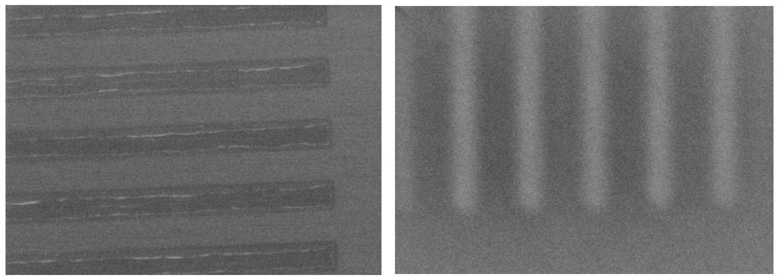
TABLE I. Plasma Doping Conditions.

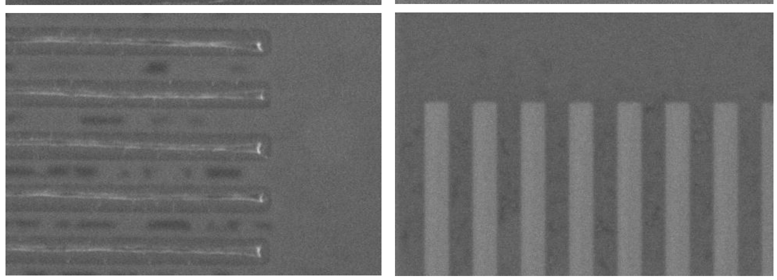
Condition	Plasma	Wafer Bias	Dose	RF Power (W)
1	B_2H_6	350V	2.00E+16	100
2	B_2H_6	350V	2.00E+15	100
3	BF_3	350V	1.50E+15	450
4	AsH_3	500V	5.00E+15	450
5	AsH_3	500V	2.00E+16	1800
6	AsH_3	500V	2.00E+16	450
7	BF_3	6kV	5.00E+16	1800
8	BF_3	6kV	5.00E+16	300

TABLE II. Post-strip SEM Pictures of Different Plasma Doping Conditions

Condition	Post AC Chemistry Dry Strip	Post dHF
1		
2		
3		
4		
5		

6 

7 

8 

Bare Si wafers (n-type for BF_3 and B_2H_6, p-type for AsH_3) were implanted with the same eight plasma doping conditions accordingly. For each doping condition, the implanted Si wafers were treated with the AC strip process developed with the patterned resist wafers implanted at the same conditions. PCOR-SIMS was used to analyze the samples pre and post strip processes. Selected SIMS profiles are shown in this paper.

For p-type wafers implanted with AsH_3 500V 5E15/cm² 450W, as shown in Figure 2, there was a 27Å Si oxide growth. Post strip dopant in the silicon was 42% less than the as-implanted sample due to the oxide growth, with some of the dopant diffused from Si to oxide.

SIMS profiles of plasma doped n-type wafers with BF_3 6kV 5E16/cm^2 1800W are shown in Figure 3. There was a very small change between the B profiles before and after the AC chemistry plasma strip, with only 8% dopant loss in the silicon The oxide growth was less than 10Å, which was much smaller than the oxide grown in oxidizing $O_2/N_2:H_2$ process.

In Figure 4, plasma doped n-type wafers with B_2H_6 350V 2E15/cm^2 100W showed shallow dopant depth in both pre and post strip samples, with 30% B dopant loss in the silicon. The oxide grew ~5Å with a notable B drop in the oxide layer after strip.

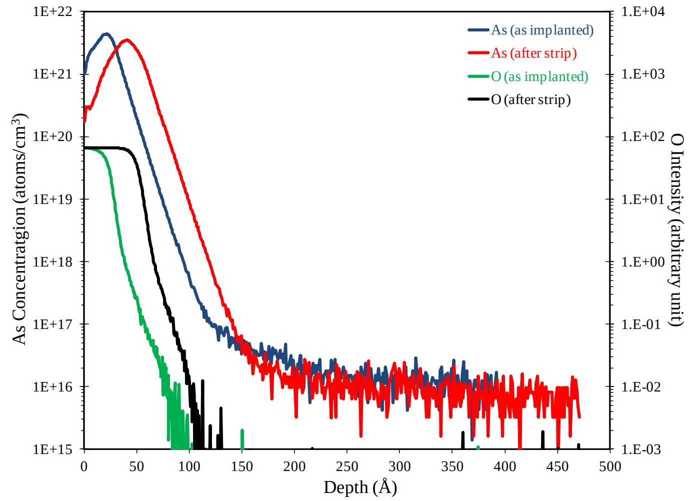


Figure 2. PCOR-SIMS depth profiles of p-type wafers plasma doped with AsH_3 500V 5E15/cm² 450W.

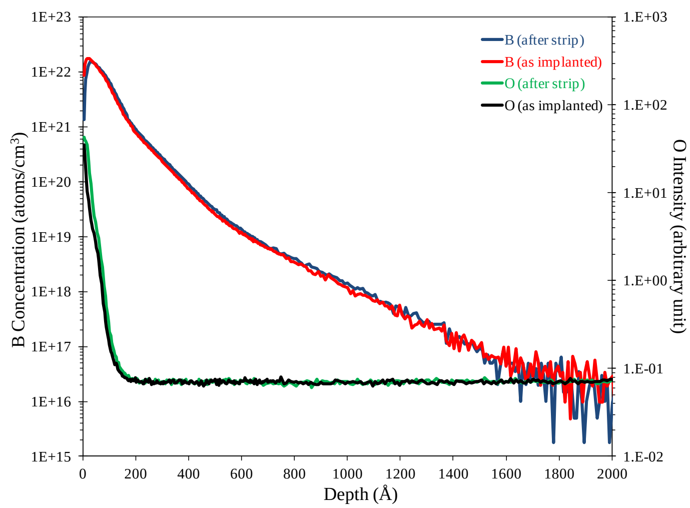


Figure 3. PCOR-SIMS depth profiles of n-type wafers plasma doped with BF_3 6kV 5E16/cm^2 1800W.

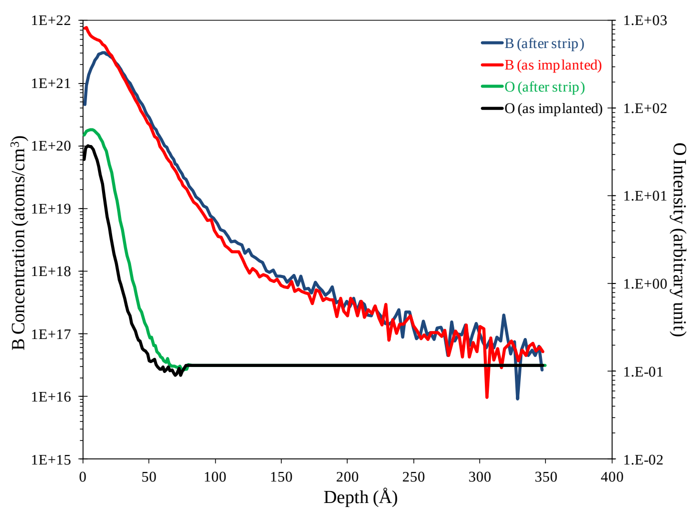


Figure 4. PCOR-SIMS depth profiles of n-type wafers plasma doped with B_2H_6 350V 2E15/cm^2 100W.

Conclusions

The study demonstrated that the AC chemistry strip processes were able to clean resist implanted with various plasma doping conditions. Compared to the convention strip processes, post strip dopant retention was improved for both n-type and p-type samples. . These processes have been tested with integrated product test wafers and shown successful results.

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